RF/MICROWAVE DETECTORS FOR EMBEDDED IC TEST

By

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RF/Microeave Detector for Embedded IC Test

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This dissertation is focused on developing embedded RFIC test circuits using the IBM SiGe processes. First, the detection theory on bipolar power detectors is analyzed in a closed-form. Then, several kinds of RF power detectors including peak detector, RMS detector and differential detector are developed. Next, two practical embedded test circuits for on-chip applications are demonstrated. One is a LNA monitoring circuit using two RF power detectors to measure LNA voltage gain and input matching. The other is a monolithic six-port reflectometer for on-chip reflection coefficient measurement. Finally, a calibration-free single-transistor detector is proposed. All above work shows that embedded RFIC test is realizable in practical application and can be a cost-effective alternative for traditional test.

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Abstract of Dissertation Presented to the Graduate School
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Manufacturing test is becoming costly with the advent of highly integrated mixed-signal circuits. Embedded IC test is very attractive as a low-cost solution and is widely used in the testing of analog and mixed-signal circuits. However, for RFIC test, embedded test is still in the infant phase in part due to the lack of the relevant high-quality on-chip detection circuits.

This dissertation is focused on developing embedded RFIC test circuits using the IBM SiGe processes. First of all, the detection theory for bipolar power detectors is analyzed in a closed-form. The detection theory includes large-signal detection, small-signal detection and RMS power detection. Then, several kinds of RF power detectors are developed. A new power detector with voltage divider enhancement is presented and compared with a Meyer power detector. The new power detector has a minimized crossover region and has a 65 dB dynamic range with $\leq 8\%$ error without calibration. A new RMS power detector is presented. It can work with signals up to 20 GHz and the dynamic range of the current design is ≥ 40 dB for

RMS power detection. Symmetric and nonsymmetric differential power detectors are developed and they both have high rejection to common-mode noise. Next, two practical embedded test circuits for on-chip applications are demonstrated. One is a LNA monitoring circuit using two RF power detectors to detect catastrophic faults or parametric faults for LNA production test. This compact LNA monitoring circuit can measure LNA voltage gain and input matching. The other is a six-port reflectometer designed to measure the microwave reflection coefficients. The six-port reflectometer consists of a resistive power divider, a phase shifter and several power detectors. It is the most area-efficient and cost-effective design for on-chip S-parameter measurement systems nowadays. This reflectometer may be used as the basis of on-chip two-port or multi-port S-parameter measurement system design in the future. Finally, the feasibility of calibration-free detector design is studied and a single-transistor detector is proposed. The single-transistor detector has less than 1% output variation with a simple DC calibration and also has self-temperature-sensing capability. The work in this dissertation shows that embedded RFIC test is realizable in practical application and can be a cost-effective alternative for traditional test.

CHAPTER 1
INTRODUCTION

1.1 Why Embedded IC Test

Due to the expanding telecommunication market as well as the markets for consumer and automotive electronics, it is becoming a recent trend to integrate various digital and analog components onto a single system-on-chip (SOC) so as to improve the performance and reduce the manufacturing cost. However, this trend brings many challenges in designing, manufacturing, testing and debugging the complex SOCs. Among them, the manufacturing test receives more attention as its cost may offset the advantage of SOCs — low cost.

It is known that the test equipment, testing time and test procedure development are three major cost factors in the current high-volume production of monolithic mixed-signal integrated circuits. The testing of analog circuits usually needs expensive automatic test equipment (ATE), consumes a long testing time and has a complicated test procedure development. So the testing of analog parts dominates the overall testing cost. For the manufacture of mixed-signal integrated circuits, the testing of analog parts takes up to 80% of the test cost while the analog modules occupy less than 10% of the total chip area [1, 2]. The situation becomes worse with higher integrated level and higher frequency of operation, especially for SOCs.

In order to minimize the production cost, the design-for-test (DfT) and built-in-self-test (BIST) techniques have recently been introduced in analog and mixed-signal circuit design [3]. These embedded test techniques migrate many external tester

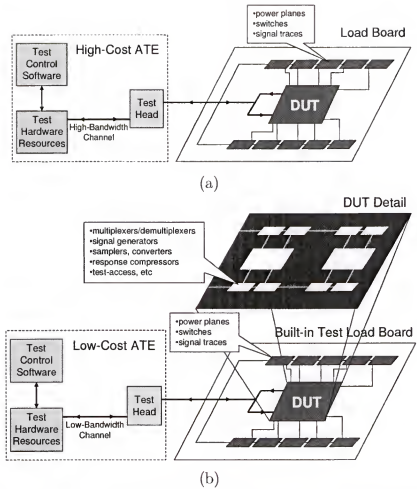


Figure 1–1: The evolution from conventional test (a) to embedded test (b).

functions to the die of the device under test (DUT) and alleviate the requirement for high-performance and thus high-cost automatic test equipment (ATE). Figure 1–1 shows the evolution from a conventional test with a high-cost ATE tester to an embedded test with a low-cost ATE tester. In a conventional test, the entire test stimulus is generated by the external testers, and the DUT response is directly relayed to it. High-bandwidth data transfer is performed at the operation speed of the DUT. However, in an embedded test, these high-speed test stimulus and response signature generation functions are handled by additional embedded circuits such as signal generators, samplers, converters, modulators, demodulators, multiplexers and

demultiplexers. The data transfer channel is, instead, utilized to send test control signals as well as low-speed test stimulus and also receive compact signatures extracted from the DUT response. Thus this channel could be a low-bandwidth connection.

Various embedded detection circuits and on-chip stimulus generators are reported in the literature [4–6]. The embedded detection circuits increase the controllability and observability of the DUT since they can access internal nodes directly without much disturbance. Moreover, the on-chip stimulus generators can provide various kinds of high-quality signals to excite the DUT for test and give more flexibility for parametric test. These embedded test techniques enable IC designers to use lower-performance DfT testers to provide IC internal node test coverage at or beyond that expected from much more expensive ATE testers. This increases test efficiency by minimizing testing time and the cost of measurement at different design and manufacturing phases, and contributes to reduced product TAT (Turn-Around-Time).

1.2 Challenges in Embedded RFIC Test

Various embedded test techniques are successfully used in the design of digital, baseband analog/mixed-signal circuits. For example, IEEE1149.1 (JTAG) boundary-scan standard [7] provides an effective means for test-access to internal modules of the DUT for testing static faults in digital ICs [8]. It has been extended to be IEEE 1149.4 [9] standard for mixed-signal testing.

However, with higher integration level and higher frequency of operation, it becomes harder to achieve the high-frequency tester functions by adding additional circuits into the DUT. That is why the high-speed embedded RFIC test lags far behind other embedded tests such as embedded tests for baseband analog circuits.

Many challenges are present in embedded RFIC test. First, RF/microwave measurement represents a completely separate discipline compared to measurement at low frequency. In the description of RF/microwave systems or components, complex values are used in the form of magnitude and phase. The scattering parameters (S-parameters), which are often used in this scenario, are complex values. Thus, the design of relevant test circuits is difficult. Second, the embedded test circuit has to be area-efficient and cost-effective. Usually, some large reactive circuits or waveguide circuits are employed for RF/microwave test. The miniaturization of such embedded circuits is very critical. Third, the high-frequency nodes in RF/microwave circuits are very sensitive to external disturbances, such as from the parasitics of attached detection circuits. A detection circuit with high input impedance is preferred because its disturbances on the DUT are minimized. In addition, a detection circuit with 50 Ω input impedance is also very useful. But then on-chip electronic switches or MEMS (micro-electro-mechanical systems) techniques are needed and may incur some additional cost. Lastly, the availability of detection circuits for a specific IC process determines the feasibility of the embedded test. For example, Schottky diode detectors in some advanced processes (i.e., GaAs) are often used in microwave measurements. But the SiGe processes and commercial silicon processes may not provide such high-quality Schottky diodes for detector design. So, the high-quality diodes or their alternatives must be developed for embedded RFIC test in the processes being used.

Even though the above challenges restrict the development of embedded RFIC test, it is still of interest to develop embedded RFIC test circuits taking into account

the tradeoffs among the costs of ATE tester, testability and chip area. As the integration level and frequencies become higher, many critical RF/microwave nodes will be unobservable and uncontrollable by today's test techniques. The lack of circuit observability and controllability can result in more design iterations, slower design time to market and inadequate manufacturing test coverage. Production test may become so difficult, slow and costly that new products may be manufactured without testing or be unprofitable to test. In this case, the embedded IC test is favored even at the expense of more chip area and more design complexity.

1.3 Approaches in Embedded RFIC Test

Failures in analog and mixed-signal circuits are commonly classified into two categories [10]: catastrophic and parametric failures. Catastrophic failures result from internal manufacturing defects like opens and shorts, while parametric failures, performance deviations from specifications, result from random variations in manufacturing process. Catastrophic failures that cause significant performance loss of the DUT can be easily detected by simple tests. However, parametric failures usually result in small deviation from nominal and are more difficult to detect. Moreover, parametric failures are more likely to occur than catastrophic failures. So, in practical IC test, the effectiveness of an analog test methodology is largely dictated by its ability to detect DUT's parametric failures.

Defected oriented tests (DOTs) and specification oriented tests (SPOTs) are the design techniques for detecting the respective catastrophic failures and parametric failures. DOTs are based on finding a suitable test signal to detect the presence of catastrophic failures using different automated fault simulation and test generation techniques [11–14]. SPOTs are concerned with a direct or indirect measurement of

the specification on the device data sheet [15–18]. Test quality metrics may be defined to evaluate or compare the effectiveness of test methodologies for a given DUT.

A variety of test approaches for embedded RF/mixed-signal IC test are reported in the literature. Some approaches borrow the ideas from traditional production test and measure the specifications on the device data sheet directly using dedicated circuits. Thus, they are classified as direct measurement. Some other approaches, however, evaluate the performance of a DUT indirectly. These approaches contain many novelties and cannot be understood intuitively, but are effective in production test. These approaches are classified as alternate testing. In the following, direct measurement and alternative testing are compared and their respective pros and cons for embedded RF/mixed-signal IC test and recent progress are presented.

1.3.1 Direct Measurement of Specifications

Traditional production test examines the functional specifications by using the appropriate tester resources and using the same kind of test stimuli and configuration with respect to which the specification is defined [19], i.e., multitone signal generator for measuring distortion, gain for codec, etc. These measurement procedures are in agreement with the general intuition of how the module behaves; thus they are conceptually simple and easy to interpret in contrast to alternative testing discussed later.

For direct measurement, embedded IC test migrates the external ATE functions into the DUT. The test of the DUT is realized on-chip by applying appropriate test stimuli and measuring the test response corresponding to the specification. [20–24] reports the implementation of on-chip signal generators and on-chip detection circuits for testing high-frequency analog circuits. The on-chip microwave signal source in

[21] can generate pure sinewave and multitone signals above the GHz range, and enable the self-testing of RF/analog blocks within the package or on the die. The on-chip spectrum analyzer in [22] can measure the spectrum of the test response using direct conversion techniques and achieve 8-bit resolution. These techniques show the embedded IC test are feasible for the in-situ measurement of high-frequency RF/analog circuits, even though the chip area taken by additional circuits is the main limitation.

Direct measurement techniques need to reconfigure the test set-up for different specification measurements. Thus, multi-specification measurements have more severe chip-area-overhead problem. Besides, longer overall test time is required for multi-specification measurements since they can not be performed simultaneously. The embedded test with direct measurement may become uneconomic due to the prohibitive costs of the additional chip area and the longer test time.

1.3.2 Alternate Test

Alternate test is a new concept proposed by A. Chatterjee [25–27]. Alternate test may be more cost-effective because alternate test uses a simpler configuration and takes less chip-area headroom than direct measurement method. Similar to the direct measurement, alternate test is to measure the DUT response to an applied test stimulus. But, the test stimuli may not be the traditional square waves or sinewaves, but an optimized transient stimulus for the predication of circuit specifications. Moreover, as shown in Figure 1–2, additional work in feature extraction and mapping from response features to circuit specifications are needed.

The fundamentals of alternate test is the mapping between specification space and measurement space. The variation in parameter space P (P is represented by

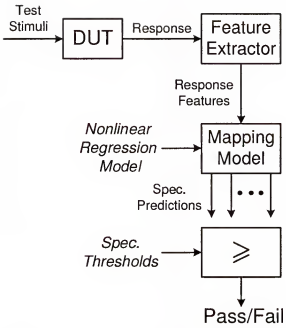


Figure 1–2: Variation in process or circuit parameter and its effect on circuit specification and test

process or circuit parameters, such as the thickness of oxide, value of a resistor, etc.), affects the circuit specification S by a corresponding sensitivity factor. Similarly, the variation in P also affects the measurement data in the measurement space M by a corresponding sensitivity factor. Figure 1–3 illustrates how the variation in P affects circuit specification in S and measurement data in M. Given the parameter space P, any point in P can be mapped onto the specification space S by $f : P \rightarrow S$ and onto the measurement space M by $f : P \rightarrow M$. Therefore, the region of acceptance in the circuit specification space has a corresponding accepted region in the parameter space. This in turn defines an accepted region in the measurement space. A faulty circuit can be found if the measurement data lies outside the accepted region in M. Alternatively, the mapping function $f : M \rightarrow S$ can be constructed using nonlinear statistical multivariate regression. Given the regression mapping from M to S, the measurement data of the DUT can predict whether the DUT is faulty or not.

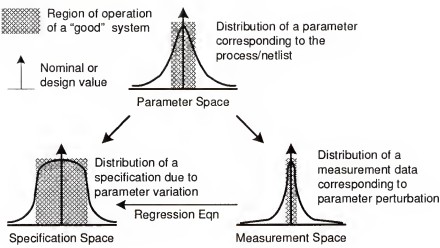


Figure 1–3: Variation in process or circuit parameter and its effect on circuit specification and test

The other key work of alternate test is to find a suitable transient test stimulus and to predicate circuit specifications accurately from alternate test response. Different test stimuli such as piecewise linear, multitone sinusoids and digital pulse trains are successfully used in the testing of op-amps, low-frequency filters, and even RF circuits [28–30]. [31] reviews recent successful applications of alternate test to RF components and addresses, in the meanwhile, that built-response acquisition in alternate testing of RF circuits is also difficult and still in the development stage.

1.4 Research Goals

The first goal of this work is to develop several kinds of on-chip RF/microwave power detectors such as peak detector, RMS detector and differential detector, using a specific IC process. Here, the SiGe process is investigated. The power detector is a device that converts RF signals to a DC output which then can be measured by low-cost DC test equipment. The power detector must have a large bandwidth and have high immunity to process and temperature variation. A power detector with a small size is preferred.

The second goal is to develop application schemes which aim at detecting functional faults in RF circuit or realizing parametric measurement by employing the above power detectors. Minimizing the chip size is still the major concern in the application schemes.

1.5 Overview of The Dissertation

This dissertation has been organized into eight chapters. The first chapter is an introductory chapter which includes an overview of embedded RFIC test, the research goals and the scope of the research work.

In Chapter 2, a complete closed-form analysis of the Meyer power detector is presented, and a new power detector is developed to minimize the crossover region and achieve a large-dynamic-range power detection. The performance of the Meyer power detector and the new power detector is compared and some issues about process variation and temperature effects are discussed in this chapter.

In Chapter 3, a closed-form analysis of the RMS power detection function in the Meyer power detector is presented and a RMS power detector design is proposed to increase the dynamic range. The new power detector can work with signals up to 20 GHz and the dynamic range of current design is ≥ 40 dB for RMS power detection.

Chapter 4 presents symmetric and nonsymmetric bipolar differential detector designs. The issue about the rejection to common-mode noise is discussed. The differential detector plays an important role in the design of a six-port reflectometer in Chapter 6.

In Chapter 5, an embedded self-test system using two RF power detectors to monitor the production of low noise amplifiers is demonstrated with an additional die area cost of 15%.

Chapter 6 is concerned with the design of a six-port reflectometer. The theory of the six-port technique and related calibration scheme are presented. An area-efficient on-chip six-port reflectometer is demonstrated to be effective for embedded RFIC test.

Chapter 7 analyzes the errors in Meyer power detector and proposes a calibration-free single-transistor detector. The emerge of this calibration-free detector makes the embedded RF IC test become feasible and practical by eliminating the costly or unpractical calibration procedure.

Chapter 8 summarizes the dissertation and presents some suggestions for the future work.

CHAPTER 2
ON-CHIP RF POWER(PEAK) DETECTORS

2.1 Overview

Current embedded RFIC testing is mainly focused on system level test (the RF-subsystem is viewed as a black box) due to the lack of a suitable on-chip RF power detector for a specific semiconductor process. However, the observation of internal nodes in RF circuits is essential for the diagnosis of the manufacturing defects. So, it is imperative to invent a desirable detector that has a large dynamic range for RF signal detection.

The BiCMOS process is very popular in the expanding wireless communication industry. Generally, it supplies high quality bipolar transistors which can be used for high frequency signal detection. A monolithic low power RF peak detector using bipolar transistors (f_T = 8 GHz) was first reported by Meyer [32]. The Meyer peak detector can be used for embedded RFIC test because it has the advantages of simplicity, wide bandwidth, low power, small chip size and temperature stability. The processes the author uses are 0.18 μm and 0.25 μm IBM SiGe BiCMOS technologies. The remarkable characteristics of the bipolar transistors in these technologies are the high β and high f_T($\geq$ 47 GHz). So, the bipolar transistor is selected as the basic rectifying element for embedded RFIC test. The author's work [33] demonstrates that the bipolar-transistor RF power detector is a promising circuit for embedded RFIC test.

The fundamental operation theory of bipolar transistor power detectors is described in Section 2.2. Besides the large-signal-detection theory [32], the small-signal-detection theory is presented to provide a bipolar transistor power detector for the large-dynamic-range signal detection [33]. The Meyer peak detector can work as a RMS detector in the small-signal detection region; thus it is also called Meyer power detector in subsequent discussions. The Meyer power detector has a drawback that its large crossover region limits its usage in large-dynamic-range signal detection. The detector crossover region is the region of operation between the detector high voltage linear and low voltage square law behaviors. It is very hard to predict input signal strength accurately in the crossover region. Therefore, a new RF power detector with voltage divider enhancement is proposed to minimize the unwanted crossover region in Section 2.3. The experimental results show the new detector minimizes the crossover region and can measure GHz signals with a 65 dB dynamic range.

2.2 Detection Theory

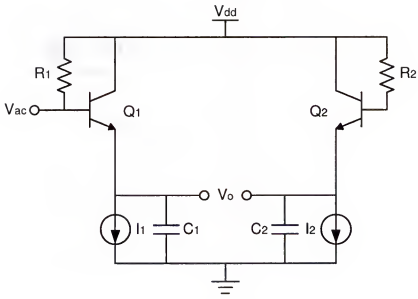


Figure 2–1: Meyer power detector (Type I) circuit.

The analysis in this section is based on the configuration of the Meyer power detector [32] as shown in Figure 2–1. The basic building block of the Meyer RF power detector is completely symmetric except for its single-ended input (V_{ac}). Bipolar transistor Q_1 rectifies the input voltage V_{ac}. Transistor Q_2 offers a DC offset voltage to balance the DC output voltage V_o to zero when the ac input signal is zero. Capacitors C_1 and C_2 filter out the ac signal and power supply noise. The DC biases of Q_1 and Q_2 should be equal so as to cancel any DC offset error whether the circuit is operated in ac coupled or DC coupled modes.

In RF power detection, the signal being detected is usually sinusoidal. The analysis of the detection principles here is therefore confined to sinusoidal signals. It is assumed in the analysis that the transistor Q_1 and Q_2 are biased identically and capacitor C_1 is large enough to ignore the decay of V_o during the negative half period of the ac input signal. The current of a bipolar transistor can be written [32] as

$$\begin{aligned} I_C &= I_S e^{\frac{V_Q}{V_T}} e^{\frac{V_{ac}\cos\omega t}{V_T}} \\ &= I_S e^{\frac{V_Q}{V_T}} [I_0(b) + 2I_1(b)\cos\omega t + 2I_2(b)\cos\omega t + \cdots] \end{aligned} \tag{2.1}$$

where V_{ac} — peak amplitude of ac input signal

V_Q — DC voltage difference of base and emitter

b — V_{ac}/V_T

$I_n(b)$ — modified Bessel function of order n [34]

From (2.1), the DC component of I_c is

$$I_{C|DC} = I_S e^{\frac{V_Q}{V_T}} I_0(b) = I_S e^{\frac{V_Q}{V_T}} \sum_{k=0}^{\infty} \frac{(\frac{V_{ac}}{V_T})^{2k}}{k!k!} \tag{2.2}$$

This equation shows the complex relationships of the DC current and the ac input-signal amplitude (V_{ac}). To simplify the analysis, approximation methods are applied.

For large values of b, $I_0(b)$ has asymptotic behavior.

$$I_0(b) \simeq \frac{e^b}{\sqrt{2\pi b}} \tag{2.3}$$

This approximation is accurate and within 8% for $b = 2$ ($V_{ac} = 50$ mV) and within 2% for $b = 6$ ($V_{ac} = 150$ mV). Let transistor Q_1 and Q_2 be identical, so that

$$I_{C1|DC} = I_{C2|DC}$$

Then we have

$$e^{\frac{V_{BE1}}{V_T}} \frac{e^{\frac{V_{ac}}{V_T}}}{\sqrt{2\pi V_{ac}/V_T}} = e^{\frac{V_{BE2}}{V_T}} \tag{2.4}$$

where V_{BE1}, V_{BE2} are the DC base-emitter voltage drops of Q_1 and Q_2, respectively. Since Q_1 and Q_2 are biased identically, $V_o = V_{BE2} - V_{BE1}$. From (2.4), the output voltage (V_o) is related to ac input-signal amplitude (V_{ac}) by

$$V_o = V_{ac} - V_T \ln \sqrt{2\pi V_{ac}/V_T} \tag{2.5}$$

This equation shows the basic principle of large-signal detection using bipolar transistors. The output voltage varies proportionally with ac input signal except for a nonlinear error term, which depends on signal strength and thermal voltage (V_T). The log function helps compress the error variance and proportionally makes the error term approximately V_T dependent. Some design strategies such as mismatching Q_1 and Q_2 and/or I_1 and I_2 can compensate for the error. However, for large-dynamic-range use (eg. $V_{ac} = 50$ mV to 1.5 V), this error term introduces a very significant

deviation, and linear regression cannot be used to predict input-signal strength accurately. The error analysis in Section 2.5 shows that the input signal should be larger than 100 mV to ensure the error is within 10% when using linear regression. A design for the removal of the signal dependent error term is proposed and will be discussed later in Section 2.3.

For small value of b, $I_0(b)$ shows the square-law behavior

$$I_0(b) \simeq 1 + \frac{b^2}{4} \tag{2.6}$$

This approximation is accurate when input signal is below 30 mV (the incident power $(P_{in}) \leq -20$ dBm for a 50 Ω system). The error is within 6% for $V_{ac} = V_T$.

Similarly, let transistor Q_1 and Q_2 be identical so that $I_{C1|DC} = I_{C2|DC}$. Then we have

$$e^{\frac{V_{BE1}}{V_T}} \cdot (1 + \frac{V_{ac}^2}{4V_T^2}) = e^{\frac{V_{BE2}}{V_T}} \tag{2.7}$$

Using $\ln(1 + x) \simeq x$, the output voltage (V_o) is expressed by

$$V_o = V_T \cdot \ln(1 + \frac{V_{ac}^2}{4V_T^2}) \simeq \frac{V_{ac}^2}{4V_T} \tag{2.8}$$

(2.8) shows the output voltage is proportional to the square of ac input-signal amplitude for small-signal detection. Also, it is seen the output is somewhat temperature dependent.

It has been shown that the detector can work in the linear region for large-signal detection ($V_{ac} > 100$ mV) and in the square-law region for small-signal detection ($V_{ac} < 30$ mV). However, there is a crossover region between linear region and square-law region in which it is hard to predict the input signal strength using simple

regression methods. The same situation exists in a Schottky diode detector [35]. Deliberate calibration using (2.2) without approximation may help improve the accuracy of the detector in crossover region, but is not easy to implement in RF/microwave on-chip test systems.

2.3 RF Power Detector with Voltage Divider Enhancement

In the subsequent discussions, Type I and II detectors refer to the Meyer power detector and a new power detector with voltage divider enhancement, respectively. For the Type I detector, a large crossover region exists between the two detection regions: linear detection for large signals and square-law detection for small signals. To combine the two signal-detection functions and make the detector work in its full range, the crossover region must be small and not introduce errors as significant as that of the Type I detector. In this section, a new RF power detector design is proposed to minimize the crossover region and realize the full-range signal detection function.

The new RF power detector design is similar to that of the Type I detector except that a fraction of the ac signal is applied to the Q_2 base. This modified design ideally eliminates the nonlinear signal dependent error term in (2.5) and realizes a linear transfer function in the large-signal-detection region. The extension of the linear-detection region and minimization of the crossover region are discussed below.

For this new detector design, identical Q_1 and Q_2 are assumed. Thus $I_{C1|DC} = I_{C2|DC}$. Let the ratioed ac input signal on the Q_2 base be ηV_{ac}, where η is a ratio of ac input signal on the Q_2 base to that on the Q_1 base. $\eta = 0.5$ is used in the following discussion of the Type II detector design and simulation.

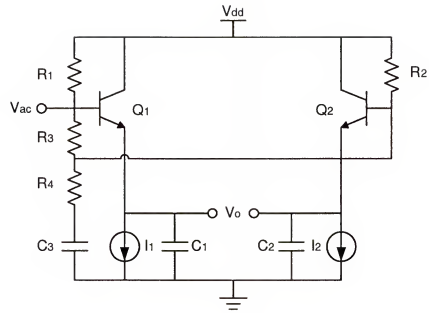


Figure 2–2: Voltage-divider enhanced RF power detector (Type II) circuit

For large-signal detection,

$$e^{\frac{V_{BE1}}{V_T}} \frac{e^{\frac{V_{ac}}{V_T}}}{\sqrt{2\pi V_{ac}/V_T}} = e^{\frac{V_{BE2}}{V_T}} \frac{e^{\frac{\eta V_{ac}}{V_T}}}{\sqrt{2\pi\eta V_{ac}/V_T}} \tag{2.9}$$

Also $V_o = V_{BE2} - V_{BE1}$. So a linear transfer function is obtained as

$$V_o = (1-\eta)V_{ac} + \frac{1}{2}V_T \ln\eta \tag{2.10}$$

As seen in (2.10), the output voltage is roughly the input signal amplitude multiplied by $1-\eta$. The second term in (2.10) introduces a small voltage offset which is independent of input signal. The error analysis in Section 2.5 shows that linear detection region is extended to 50 mV with an error below 2%.

For small-signal detection, it is easy to show that the output voltage is still proportional to the square of the ac input-signal amplitude. However, the output voltage is $1-\eta^2$ times of that of the Type I detector at the same input signal. The

output voltage for small-signal detection is given by

$$V_o \simeq \frac{(1-\eta^2)V_{ac}^2}{4V_T} \tag{2.11}$$

The simulation and experimental results in Section 2.5 show that the detector still operates in the square-law region below 30 mV with error less than 2%. The intercept of linear and square-law region is at 40 mV and the crossover region is minimized to $30 \sim 50$ mV input levels. Moreover, the narrow crossover region can be modeled as either linear or square-law behavior with an error below 8%.

2.4 Circuit Implementation

Both Type I and Type II RF power detectors have been designed using 0.25 μm IBM6HP and 0.18 μm IBM7WL BiCMOS technologies. The Type I detector is shown in Figure 2–1. A single-ended ac input signal is only applied to the base of transistor Q_1. Q_1 rectifies the ac input signal and C_1 lowpass filters all unwanted ac harmonics. Q_2 provides a DC output voltage to cancel the DC offset. The DC voltage difference between the emitters of Q_1 and Q_2 indicates input-signal strength using either (2.5) or (2.8). The current sources are identical. Bipolar transistors with high V_A are chosen to implement the current sources so that the non-ideality of the current sources due to Early effect is negligible. The output voltage droop ΔV_o is given by

$$\Delta V_o = -\frac{I}{C}\Delta t \tag{2.12}$$

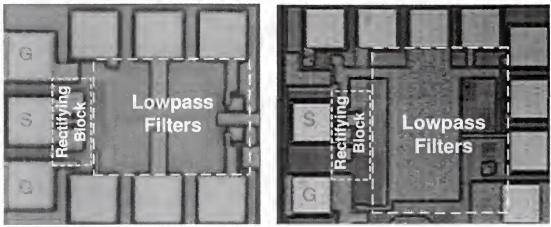
where Δt is approximately half the period of the ac input signal. To reduce ΔV_o, the bias currents (I_1, I_2) and capacitor C_1 are set to 20 μA and 40 pF, respectively.

The new Type II RF power detector shown in Figure 2–2 has one extra voltage divider at the input. The ratio of this divider is 1 : 2, thus it provides half the input

signal to the Q_2 base. The remaining rectifying cell is identical to that in the Type I detector.

In both designs, noise and signal coupling are critical issues since the detectors work with GHz signals. Beside C_2, which is used to filter power supply noise, other bypass capacitors are needed on critical nodes such as V_{dd}, the base of Q_2 (Type I detector), etc. Signal-coupling reduction and noise isolation are dealt with in the design/layout.

2.5 Simulation and Experimental Results



(a) (b)

Figure 2–3: Chip photos of (a) Type I detector (600×550 μm^2) and (b) Type II detector (720×550 μm^2)

Figure 2–3 shows the chip photos of the Type I detector and Type II detector. They both were fabricated using 0.25 μm IBM6HP BiCMOS process. The chip size of these two detectors are 600×550 μm^2 and 720×550 μm^2, respectively, including the bondpads and the chip edge. As seen in Figure 2–3, the rectifying block consists of a couple of rectifying bipolar transistors and the corresponding bias current sources and takes a small portion of the chip area while the lowpass filters and bondpads occupy more than 80% of the chip area.

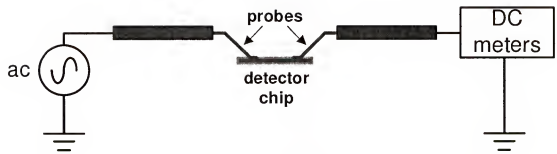


Figure 2–4: Test set-up for the characterization of RF power detector

The characterization of a power detector is a complicated process. The basic set-up for characterization is shown in Figure 2–4. A RF signal from an off-chip signal source is fed into a power detector through a coaxial cable and Cascade Microtech microwave probe. Then a set of DC voltage meters are used to collect the DC voltages of the power detector at the output. To obtain the transfer characteristics of the DC output voltage (V_o) versus input ac signal (V_{ac}), the input absolute power or voltage should be known. However, the losses of the cable and the microwave probes decrease the incident power. The input matching, which is realized by a shunt on-chip 50 Ω resistor, also has an effect on the input voltage. So a systemic calibration is built up to calculate the input signal strength. The calibration scheme based on a one-port error model is presented in the Appendix A.

The Type I and Type II detectors have similar frequency response since the Type II detector only adds an extra resistive voltage divider on the Type I detector. At the input, except for a 50 Ω resistance, there is a small parasitic capacitance ($\approx$ 32 fF) which is introduced from the base of the bipolar transistor. Only two transistors of minimum size are used as the basic rectifying element in both detector designs. So both detectors have good high frequency performance. Figure 2–5 shows the frequency response of the Type I detector, which is simulated with 1 V ac input

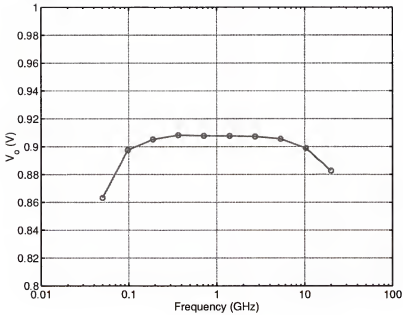


Figure 2–5: Frequency response of RF power detector

signal. It exhibits a flat frequency response from 100 MHz to 10 GHz. At frequencies above 10 GHz, the output voltage drops quickly with frequency. This is due to loss via r_b, parasitic capacitance in the bipolar transistor and the ac coupling capacitor at the input. At low frequencies, the sharp drop of output voltage illustrates that the circuit loses accuracy below 80 MHz which is due to the small input ac coupling capacitor. A bigger input capacitor can be used to expand the low frequency bandwidth.

Figure 2–6 shows the comparison of Type I and Type II detector transfer characteristics at 5.2 GHz. Both the simulated and measured results are shown in the same plot. It is seen that the measured results agree with the simulation for both detector types. Even though the curves of both detectors have a reflected point in -10 dBm ~ -20 dBm where the crossover region is, it is hard to tell the Type II detector has improved performance in the crossover region compared to the Type I

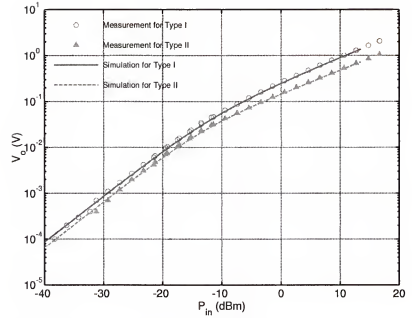


Figure 2–6: Comparison of Type I and Type II detector transfer characteristics

detector. Thus another figure focusing on the crossover region is plotted in Figure 2–7. As shown in Figure 2–7, the fitting line from the linear region is almost continuous with that from the square-law region for Type II detector. However, there is a sharp discontinuity at 50 mV between the fitting lines from the linear region and from the square-law region for the Type I detector. Moreover, the analysis of the respective relative errors for both detectors is illustrated in Figure 2–8. The Type II detector has a flat near-zero-relative-error curve in the whole detection region while the Type I detector has a large error in the crossover region around 30 mV to 100 mV. For the Type II detector, the errors in both the linear region and the square-law region are below 2% by either (2.10) or (2.11). The error in the crossover region is below 8% if estimated by either (2.10) or (2.11). So the Type II detector can be used to detect signal level between -50 dBm to 15 dBm without the need of any complicated

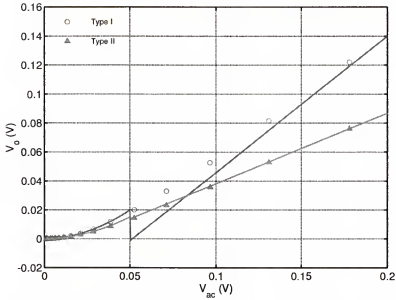


Figure 2–7: The deviation in the extrapolation of the transfer characteristics of Type I and Type II detectors.

calibration scheme. However, for the Type I detector, a deliberate calibration scheme for the large crossover region is required to expand its application.

2.6 Discussion

The functionality of the Type I and the Type II detector has been demonstrated in the previous sections. However, some issues must be considered seriously for embedded test in an industrial application. Therefore, the DC bias, process variation and temperature variation issues are discussed in the following section.

First, the DC bias should be clean in some sensitive nodes like the base of rectifying bipolar transistor. In the design discussed before, the base of bipolar transistor is connected with DC supply source V_{dd} through a large resistor. The power source may introduce some noise to the base. So to avoid the risk of unwanted noise effects, the base of rectifying transistor is best biased by a clean off-chip DC source.

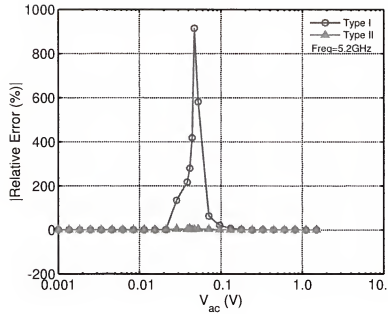


Figure 2–8: Comparison of the relative errors for the Type I and Type II detectors.

Second, the process variation is an important issue for industrial applications. The performance change due to the process variation and mismatch is investigated by running a Monte Carlo simulation. The detector with on-chip current sources is simulated with a 5.2 GHz 100 mV input ac signal and it shows a 6% variation of output value. However, the simulation with ideal current sources in Chapter 7 shows less than 1% variation of output value. This indicates that a calibration-free detector can be developed for industrial applications. The third is the temperature effect. Generally, the Type I and Type II power detectors have different responses to temperature variation in the large-signal-detection region and small-signal-detection region. The detectors have more stable performance in the large-signal-detection region than in the small-signal-detection region. The compensation for small-signal detection in Chapter 7 is complex and needs a calibration procedure similar to temperature measurement. In contrast, for large-signal detection, the compensation is

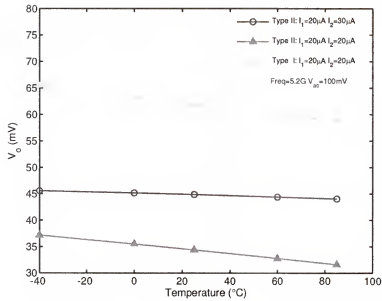


Figure 2–9: Comparison of the temperature effects for the Type I and Type II detectors.

easy or even not needed. It is worth reporting that a simple bias adjustment can make the detector have more immunity to temperature variation for the large-signal detection. For example, it is easily proved that the Type II detector performance can be independent of the temperature effect if $I_1/I_2 = \sqrt{\eta}$, where I_1 and I_2 are the respective DC biases on the left and right legs as seen in Figure 2–2. Figure 2–9 is the simulated temperature response of Type I and Type II detectors in various bias conditions. The simulation is performed with a 5.2 GHz 100 mV sinusoid signal. The figure illustrates that the temperature response of the Type II detector with $I_1 = 20$ μA and $I_2 = 30$ μA looks like a horizontal straight line while the other two have an apparent oblique slope. The temperature coefficients are -0.055 mV/°C for Type I detector with both 20 μA biases, -0.045 mV/°C for Type II detector with both 20 μA biases and -0.012 mV/°C for Type II detector with $I_1 = 20$ μA and $I_2 = 30$ μA.

2.7 Conclusion

A RF power detector using bipolar transistors has three detection regions: linear, square-law and crossover region. Both linear and square-law detections are highly accurate. But the input-signal strength is extracted inaccurately in the crossover region. The Type I detector [32] has a wide crossover region which limits its usage in large-dynamic-range-signal detection. The proposed Type II detector minimizes the crossover region to 30 $\sim$ 50 mV and can work with a 65 dB dynamic range. The errors in linear and square-law regions are within 2% and the error in crossover region is within 8% using either linear or square-law estimation. The process variation analysis shows the detector has less than 1% output variation if using matched current sources. The temperature effect analysis shows temperature effects can be eliminated by some temperature compensation scheme. Above all, the power detector using bipolar transistors is a prospective candidate circuit for embedded RFIC test.

CHAPTER 3
RF RMS DETECTORS

3.1 Overview

In the preceding chapter, a RF power detector for pure sinusoid signal detection is discussed. However, in some cases such as the power control of a transmitter, multi-tone test, electromagnetic interference(EMI) measurement, etc, it is more necessary to know the RMS value of the total power than the peak power. This is because the RMS power is a useful, consistent and standard way to measure and compare dynamic signals despite of their variation in shape and size. For embedded RFIC test, an area-efficient RMS detector is necessary to convert on-chip high frequency signals to baseband signals, which then can be measured by low-cost baseband test equipment.

RMS detector of various designs are reported in the fields of communications and of measurement systems. Thermal-based, diode-based and translinear-based detection methods are well-known in the design of RMS power detectors. Thermal-based detectors first convert ac power to thermal power by using resistive components and then measure the ambient temperature change which is proportional to the thermal power or the dissipated ac power [36]. These kinds of detectors have the advantages of wide bandwidth and good accuracy. However, chip-level implementation is complicated by thermal coupling among adjacent circuits through the substrate. Diode-based detectors employ the square-law detection characteristic of diodes [35]. Diode detectors are widely used in communication systems for power measurement

because of their favorable high frequency performance and low cost. However, diode detectors are temperature-dependent and have limited dynamic range, so elaborate compensation techniques are required to make those detectors operate as true RMS detectors. Moreover, RF/microwave high-quality diodes such as Schottky diodes are unavailable in many advanced semiconductor processes. Translinear-based detectors employ the translinear principle, which is based on the exponential law describing the large-signal behavior of the bipolar transistor or the MOS transistor operating in the weak inversion region [37–39]. The principle of operation is that an input ac voltage is converted to a current signal using a V-I converter, squared by a squarer-divider and then put through a low-pass filter to produce a DC output which is proportional to the power of the input signal. The input interface (V-I converter) restricts use of these circuits above 1 GHz due to its limited bandwidth. A translinear detector with bandwidth up to 1 GHz was recently developed [37] using BiCMOS technology. Translinear-based detectors have limited bandwidth compared to thermal-based or diode-based detectors.

Embedded test requires using existing processes without any modification that incurs the cost increase on the mask. For the process being used, the above mentioned RMS detector designs are not feasible due to the unavailability of high quality diode, complexity and bandwidth limitations. The discussion on power detectors in Chapter 2 demonstrates that the bipolar transistor is a promising element for power detection. In fact, the transfer characteristics of the bipolar power detectors in Chapter 2 are very similar to those of diode power detectors. Thus, bipolar transistors may replace diodes for realizing RF/microwave RMS power detection. With this idea, an in-depth investigation [40] is done on the RMS detecting function of Meyer

power detectors [32]. Section 3.2 analyzes the operating principle of RMS detection of Meyer power detectors and shows Meyer power detectors are equivalent to diode detectors, which are widely employed in communication and microwave measurement systems. Section 3.3 describes an RMS detector design using a cascaded attenuation structure to achieve high dynamic range. Section 3.4 shows some issues about circuit implementation and some simulation and experimental results.

3.2 RMS Detection Analysis

The analysis in this section focuses on the square-law detection characteristics of a Meyer power detector as shown in Figure 2–1. In contrast to the analysis in the preceding chapter, the input signal here is allowed to be a periodic signal of any shape instead of a pure sinusoid signal. The input periodic signal can be represented as the sum of N harmonics, where N is a positive integer.

$$V_{ac} = \sum_{i=1}^{N} V_{ac_i} cos(\omega_i t + \phi_i) \tag{3.1}$$

where V_{ac_i}, ω_i and ϕ_i are the peak amplitude, angular frequency and phase of the i-th harmonic. Thus, the current in transistor Q_1 is expressed as

$$I_{C1} = I_S e^{\frac{V_{BE1}}{V_T}} \cdot \prod_{i=1}^{N} e^{\frac{V_{ac_i} cos(\omega_i t + \phi_i)}{V_T}} \tag{3.2}$$

where V_{BE1} is the DC base-emitter voltage of transistor Q_1 and V_T is the thermal voltage.

Similar to (2.1), the above equation can be written as

$$I_{C1} = I_S e^{\frac{V_{BE1}}{V_T}} \prod_{i=1}^{N} [I_0(b_i) + 2I_1(b_i)\cos(\omega_i t + \phi_i) + 2I_2(b_i)\cos(\omega_i t + \phi_i) + \cdots] \tag{3.3}$$

where $I_n(b_i)$ is modified Bessel function of order n [34] and $b_i = V_{ac_i}/V_T$. It is seen in (3.3) that each harmonic (i.e., i-th harmonic) produces a DC component $I_0(b_i)$ and other ac components. The total current I_{C1} depends on all of the harmonics. Since $\omega_i \neq \omega_j$, $\forall i \neq j$, cross-modulation among them does not produce any DC component. Thus the DC current component of I_{C1} can be viewed as the result of DC components produced by the corresponding harmonics.

Using the approximation in (2.6) for small signal detection, the DC component in I_{C1} can be simplified as

$$I_{C1|DC} \simeq I_S e^{\frac{V_{BE1}}{V_T}} \prod_{i=1}^{N} (1 + \frac{V_{ac_i}^2}{4V_T^2}) \tag{3.4}$$

Similarly, assuming transistor Q_1 and Q_2 are identical, so that $I_{C1|DC} = I_{C2|DC}$,

$$e^{\frac{V_{BE1}}{V_T}} \prod_{i=1}^{N} (1 + \frac{V_{ac_i}^2}{4V_T^2}) = e^{\frac{V_{BE2}}{V_T}} \tag{3.5}$$

Using $\ln(1 + x) \simeq x$ and $V_o = V_{BE2} - V_{BE1}$, the output voltage (V_o) is expressed by

$$V_o = V_T \cdot \sum_{i=1}^{N} ln(1 + \frac{V_{ac_i}^2}{4V_T^2}) \simeq \frac{1}{4V_T} \sum_{i=1}^{N} V_{ac_i}^2 \tag{3.6}$$

This equation shows that the output voltage is linearly proportional to the sum of the square of all harmonics' amplitudes, which corresponds to the total power. Also, it is seen that the output is somewhat temperature dependent. So the temperature compensation technique in Chapter 7 is needed.

The above derivation is restricted in the square-law small-signal-detection region. The dynamic range of the detector is very limited. It is necessary to increase the dynamic range for the application in embedded test. Section 3.3 will discuss the extension of dynamic range.

3.3 Proposed RMS Detector Design

The preceding section shows that the Meyer power detector can measure RMS power in the small-signal-detection region. Simulations show that 20 GHz RF/microwave RMS power detection with approximately 20 dB dynamic range is achievable using the IBM 7WL process. However, for embedded test, a larger dynamic range is needed. To extend the dynamic range, we could cascade several constant-gain amplifier stages or several constant-gain attenuators. In our RMS detector design, attenuators are used to extend the dynamic range of detection for the following reasons:

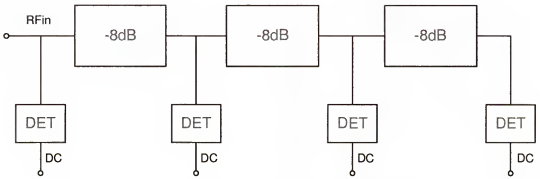


Figure 3–1: Block diagram of proposed RMS detector.

1. A wideband constant-gain amplifier is not available in the GHz frequency range. In addition, the cascaded structure limits its high frequency performance.
2. Unlike an amplifier, an attenuator is a wideband, area-efficient and easily integrated component. Only passive resistors are used in our attenuator design. An attenuator with a constant gain up to 20 GHz can be easily achieved. Monte Carlo simulations with the IBM 7WL process shows the variation of attenuation

is only ±0.08 dB with process variation, mismatch and temperature. Thus a resistive attenuator is almost an ideal component for the dynamic-range extension of the detector.

3. A single Meyer power detector has a small dynamic range and is only suitable to detect RMS power with signal level below 40 mV. However, the signal strength in RF testing is commonly in the range of several millivolts to several hundred millivolts. So the attenuator is needed to reduce the signal strength to the range that the RMS detector can detect accurately.

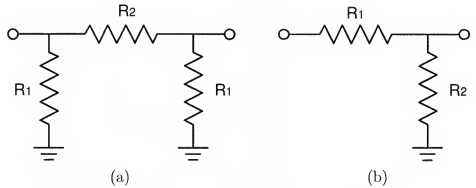


Figure 3–2: The configuration of (a) π-type attenuator and (b) 50 Ω L-type terminator

The RMS detector in Figure 3–1 has 3 stage 8 dB attenuators in series, a BJT detector (the left half of Meyer power detector in Figure 2–1) at the input and output of each attenuator and an extra BJT detector (not shown in Figure 3–1) which is used as the reference for all detectors (the right half of Meyer power detector in Figure 2–1). The first two stage attenuators are π-type resistive attenuators as shown in Figure 3–2(a). They have a symmetrical structure that is matched to 50 Ω on both sides. The last or the third attenuator is a 50 Ω terminator consisting of two resistors in series as shown in Figure 3–2(b). The last attenuator reduces voltage signals by 8 dB while working as a terminator.

For a given input signal, there are four DC outputs along the attenuation line. Due to the limited dynamic range of the detectors, no more than two detectors at a time can operate in the optimal detection range. These are the detectors whose outputs should be used to estimate the input power. Here, we present a scheme for finding which detectors are working in the optimal detection range. The ratio of the input and output powers of a constant-gain attenuator should be a constant. If the RMS detectors at the input and output of an attenuator are both in the optimal range, the ratio of their output voltages should equal the gain of attenuator. Otherwise, the ratio of their output voltages will not equal the gain of attenuator. So, to find the detectors working in the right range, the ratios of consecutive outputs should be compared. The ratio which best approximates the attenuator gain tells us that the corresponding detectors are the best ones to use to estimate the RMS power. Figure 3–3 shows the flow graph to select the appropriate detector and estimate the input RMS power. The RMS detectors give four DC outputs: V_1, V_2, V_3 and V_4. Then we have $A_{V_1}(V_1/V_2)$, $A_{V_2}(V_2/V_3)$ and $A_{V_3}(V_3/V_4)$. If the i-th value $A_{V_i}, i \in [1, 2, 3]$ is the closest to the ideal attenuator gain, the corresponding detector outputs V_i and V_{i+1} should be used to estimate the input RMS power. Assume the relation between output voltage (V_o) and input RMS power (P_{in}) of a detector is $V_o = \gamma P_{in}$, where γ is a constant. Then the input RMS power (in dBm) to the whole detector is $\frac{V_i}{\gamma} - (i-1)G_a$ by using V_i or $\frac{V_{i+1}}{\gamma} - iG_a$ by using V_{i+1} or the average of the above two, where G_a is the attenuator gain.

The absolute value of attenuator gain (in dB) has to be no more than a half of the dynamic range of each detector to ensure that at least two consecutive detectors

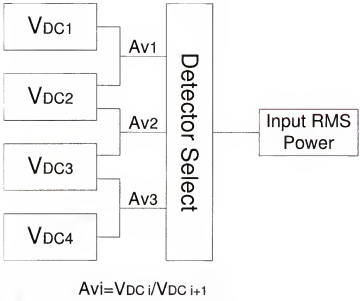


Figure 3–3: Estimation of input RMS power.

are in the optimal detection range. Our RMS detectors have at least 16 dB dynamic range, so the gain of the attenuator was set to -8 dB.

It can be seen in Figure 3–1 that the first detector accesses the input signal directly and acts as a peak detector for large signals as an RMS detector for signals within the optimal signal range [32,33]. The relation of output voltage (V_o) and input ac signal (V_{ac}) in large-signal peak detection mode is [32]

$$V_o = V_{ac} - V_T \ln \sqrt{2\pi V_{ac}/V_T} \tag{3.7}$$

Thus this detector could be called an RF peak/RMS detector.

3.4 Simulation and Experimental Results

The RF peak/RMS power detector circuit was fabricated using IBM 7WL Bi-CMOS process. A micrograph of the IC is shown in Figure 3–4. The chip size is 700×550 μm^2 including all ac and DC bondpads. Except for the bondpads, most of the chip area is occupied by low-pass capacitors (30 pF MOS capacitor at

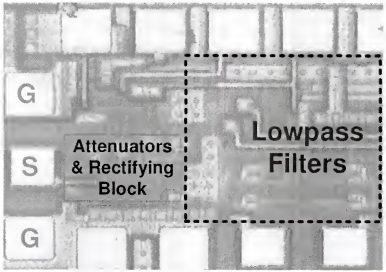


Figure 3–4: Chip photo of RF peak/RMS power detector ($700 \times 550\ \mu m^2$).

each detector output). The single detector design is similar to the Meyer power detector design in Chapter 2 except that the base biases of the BJTs are connected with a clean external DC source instead of the noisy circuit power supply. The modified DC biases in Figure 3–5 help to reduce power supply noise effects in the applications in embedded test. Both components Q_1 and Q_2 use two minimum-size bipolar transistors considering the symmetry of layout and the degradation of input matching. The input reflection coefficient of this design is -16 dB at 20 GHz. A large on-chip bypass capacitor (12 pF in this design) is put on the power supply to suppress power supply noise induced by the detectors. The noise spike at the power supply is less than 2 mV, so the detectors have negligible effect on the circuit-under-test. The resistors in the attenuator and terminator design are formed by the K1 layer. The K1 layer is located between the metal1 and metal2 layer and has 64.85 Ω sheet resistance. Simulation shows the attenuator and terminator have small variation of loss at high frequency and ± 0.08 dB variation considering process, mismatch and temperature

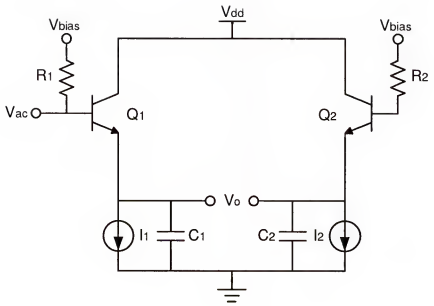


Figure 3–5: Meyer power detector with modified biases.

variation. The attenuator and terminator in the detector design have 8 dB loss. The resistances R_1 and R_2 in Figure 3–2 are given by (3.8) for the attenuator and by (3.9) for the terminator.

$$\begin{aligned} R_1 &= Z_0 \left[\frac{10^{\frac{A}{20}} + 1}{10^{\frac{A}{20}} - 1} \right] \\ R_2 &= \frac{Z_0}{2} \left[\frac{10^{\frac{A}{20}} - 1}{10^{\frac{A}{20}}} \right] \end{aligned} \tag{3.8}$$

$$\begin{aligned} R_1 &= Z_0 - R_2 \\ R_2 &= Z_0 10^{-\frac{A}{20}} \end{aligned} \tag{3.9}$$

where $Z_0 = 50\ \Omega$ and A is the attenuator loss or voltage divided ratio in the terminator. Here, A is 8 dB.

The RMS power detection function was verified through simulations. Figure 3–6 shows DC voltage output (V_o) versus ac input (V_{ac}) in the square-law-detection region

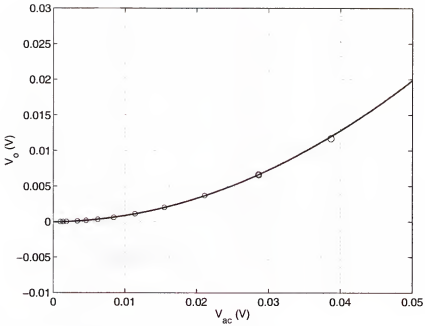


Figure 3–6: Square law detection of a single detector.

of a single detector. The solid line represents a 2^{nd}-order fit expressed by $V_o = \gamma V_{ac}^2$, where γ is a constant. Measurements in Chapter 2 demonstrated square-law behavior in a single detector for frequencies up to 10 GHz. Measurements of a newly designed detector with 20 GHz sinewave inputs are shown in Figure 3–7. In the square-law detection region, the slope reflects the required quadratic behavior. The slope in the linear detection region is less than that in square-law region and represents near-linear behavior as predicted by (3.3). Measurements show that the detector works well at or above 20 GHz. The performance of this bipolar detector is superior to that of most diode detectors.

Figures. 3–6 and 3–7 represent results for pure sinusoidal signals. However, as a RMS detector, the circuit should have consistent response for signals having equal powers but various waveform shapes. Thus, simulations using various waveforms were done to verify the RMS power detection function of each detector. The simulated

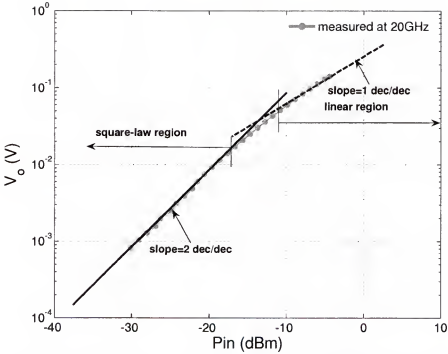


Figure 3–7: Measured transfer characteristics of a single detector.

detector responses to two-tone signals, square waves and triangular waves are compared with the response to a single-tone sinusoid signal as shown in Table 3–1. The single-tone signal is a 5.2 GHz sinewave. The two tones were at 5.2 GHz and 5.25 GHz. Both the square and triangle waves are at 5.2 GHz. It is seen that the errors are below 4% for $V_{ac} \leq 30$ mV and below 5.5% for $V_{ac} \leq 40$ mV.

The new RMS detector was measured with 5.2 GHz signals. Figure 3–8 shows the DC outputs from the four detectors along the attenuation line. The solid lines represent the transfer characteristics of the four detectors for RMS power detection. The solid lines have equal slopes and are equally distributed horizontally. The horizontal distance between two consecutive lines is 8.08 dB, which almost equals the measured attenuator loss of 8.16 dB as seen in Figure 3–9. The overlap of the solid lines in Figure 3–8 shows that the dynamic range for RMS power detection is larger

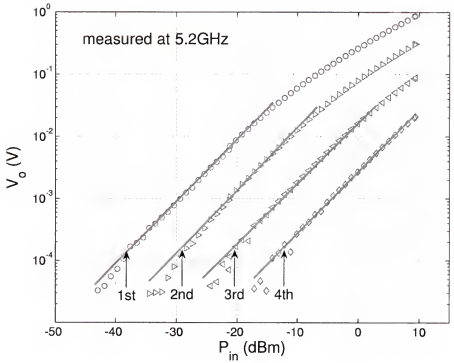


Figure 3–8: Measured transfer characteristics of the new RMS detector.

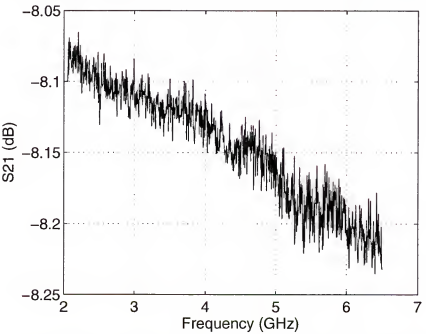


Figure 3–9: Measured S21 of the attenuator using a network analyzer.

Table 3–1: The simulated response of a single detector to various waveforms.

Equivalent	1 tone	2 tones		Square Wave(50%)		Triangle Wave	
Input(mV)	V_o(mV)	V_o(mV)	Error(%)	V_o(mV)	Error(%)	V_o(mV)	Error(%)
5	0.238	0.236	-1.14	0.230	-3.46	0.231	-2.97
10	0.928	0.929	0.14	0.908	-2.10	0.909	-2.01
15	2.068	2.083	0.71	2.013	-2.65	2.061	-0.33
20	3.624	3.670	1.29	3.511	-3.10	3.631	0.21
25	5.562	5.678	2.11	5.362	-3.58	5.598	0.67
30	7.828	8.093	3.38	7.515	-4.00	7.858	0.38
35	10.419	10.869	4.32	9.936	-4.64	10.444	0.24
40	13.267	13.981	5.38	12.574	-5.23	13.334	0.51

than 40 dB. The characteristics at higher power levels can be used for peak power detection.

3.5 Conclusion

Closed-form analysis shows that the classic Meyer peak-detector circuit can also be used for RMS detection, although over a limited dynamic range. In a new detector implementation, several stages of resistive attenuators are employed to extend the dynamic range. Moreover, a scheme is developed to estimate the input power from a series of DC outputs. The proposed detector can still realize RF peak detection since the first detector accesses the input signal directly. The new power detector can work with signals up to 20 GHz and the dynamic range of current design is at least 40 dB for RMS power detection.

CHAPTER 4
RF DIFFERENTIAL DETECTORS

4.1 Overview

The trend of substituting differential circuits for single-ended circuits happens because the differential circuits have the advantages of high rejection of common-mode noise, high output swing and high linearity compared to the single-ended alternatives. So it is essential to invent a circuit to detect differential signals for embedded test application. A truly differential detector must have the capability to detect the difference of two signals of interest. The detection of a differential signal cannot be achieved simply by detecting the opposite signals using two single-ended power detectors. It is easily proven as below.

Given the signals i and j are represented by

$$V_i = A\cos(\omega t + \phi_i) \tag{4.1}$$

$$V_j = B\cos(\omega t + \phi_j) \tag{4.2}$$

Thus, the difference of the two signals is

$$V = V_i - V_j = \sqrt{A^2 + B^2 - 2AB\cos(\phi_i - \phi_j)}cos(\omega t + \psi) \tag{4.3}$$

where, $\psi = \cos^{-1}(\frac{A\cos\phi_i + B\cos\phi_j}{\sqrt{A^2 + B^2 - 2AB\cos(\phi_i - \phi_j)}})$.

The amplitude of V is determined by A, B and $\phi_i - \phi_j$. The single-ended detectors can measure the two signals' amplitudes, A and B but cannot give any

information about the phase difference $\phi_i - \phi_j$. So the differential signal detection cannot be achieved using two single-ended detectors.

The traditional approach for differential signal detection is to convert the differential signal to a single-ended signal and then process it by conventional single-ended detection circuitry. The balun is widely used for the conversion of differential signal to single-ended signal at high frequency. However, the inductive balun is not area-efficient for on-chip implementation. A V−I converter which can convert a differential voltage signal to a proportional current signal is employed for high frequency differential detector design. However, the V−I converter has a limited bandwidth [37]. So the traditional approaches are not suitable for embedded RFIC test.

A simple diode-type differential detector was developed in [41]. As shown in Figure 4–1, a differential signal is applied directly to the base and emitter of the diode, rectified by the diode junction and then filtered by a low-pass structure formed by the capacitor C_F and the resistor R_F. The merit of high input impedance is still maintained either from the base or emitter by employing a small bias current. A similar alternation on Meyer power detector can also achieve the function of differential signal detection. In this chapter, we present two differential-signal detectors using bipolar transistors, compare their performance and demonstrate their high rejection to the common-mode noise.

4.2 Differential Detector Design

There are two approaches to design RF/microwave detector. One is to have the input impedance of the detector as high as possible so that the detector has a negligible disturbance on the performance of the device under test (DUT). The other one is to make the detector match to a 50 Ω system so that the detector can work

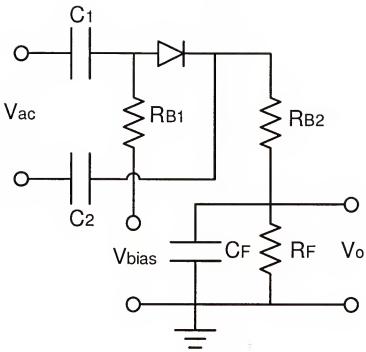


Figure 4–1: Diode differential detector circuit.

as a terminator of a DUT while it detects the output of the DUT. Usually the first approach is preferred in embedded RFIC test.

In this differential detector design, the bipolar transistor is used as the rectifying element. The impedance seen into the base of bipolar transistor is very high and the impedance into the emitter is about $1/g_m$, where g_m is the transconductance of the bipolar transistor. Because the input impedance into the emitter is inversely proportional to the bias current, the high input impedance can be achieved just by using a small bias current. So a differential detector which has high input impedances can be realized just by applying the differential signal to the base and emitter of a bipolar transistor directly.

Similar to the diode differential detector in Figure 4–1 [41], a bipolar differential detector is implemented as shown in Figure 4–2 (replica reference circuit is not shown).

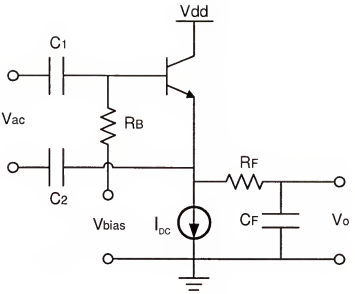


Figure 4–2: Bipolar differential detector circuit.

A differential signal is applied to the base and emitter of a bipolar transistor which has a small bias current ($I_{bias} = 20\ \mu A$); then the signal is rectified by a bipolar transistor and filtered by an RC low-pass filter. The two capacitors C_1 and C_2 are used to decouple the DC voltage of DUT from the detector. The resistor R_B is to isolate high frequency signals from the bias DC source. The resistor R_F and capacitor C_F form a low-pass filter at the output. The principle of differential detection is similar to that of single-ended signal detection so the detection theory can be referred to Chapter 2.

The differential detector mentioned above does not have a symmetric structure. It may cause a little disturbance on the performance of a completely symmetric circuit under test. So a new version of differential detector having a completely symmetric structure is proposed in Figure 4–3 (replica reference circuit is not shown). Four ac-coupled capacitors are used at the differential input. The two bipolar transistors at the center are to rectify the ac differential signal. A low pass filter at the output

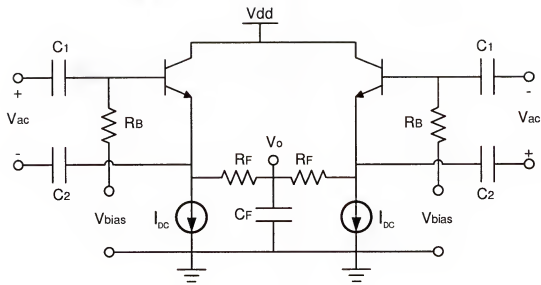


Figure 4–3: Symmetric bipolar differential detector circuit.

is formed by the resistors R_F and the capacitor C_F. The output node of this filter is a virtual ground since the differential detector is completely symmetric. So the detector has smaller ripples at the output and much shorter settling time than the nonsymmetric counterpart in Figure 4–2. However, the symmetric detector consumes more power and takes more area than the nonsymmetric counterpart in Figure 4–2.

4.3 Simulation

Both the symmetric and nonsymmetric differential detectors are compared in the simulations using IBM 7WL BiCMOS process. Figure 4–4 shows the transfer characteristics of the symmetric and nonsymmetric bipolar differential detectors simulated with a completely differential signal at 5.2 GHz (180° phase difference for signals into the base and emitter). It is seen both detectors have an almost identical transfer characteristics as the Meyer power detector discussed in Chapter 2.

For the nonsymmetric differential detector, the input impedances to the base and emitter of the BJT have a small difference. The simulated base input impedance is

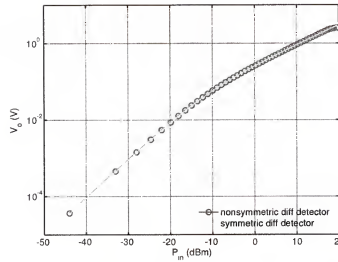


Figure 4–4: The simulated transfer characteristics of the symmetric and nonsymmetric bipolar differential detectors.

1.2 kΩ and the emitter input impedance is 900 Ω. The impedance difference has little impact on the DUT performance since the base and emitter of the BJT are connected to the nodes with 50 Ω impedance. To verify the differential signal detection function, the nonsymmetric detector is simulated by varying the amplitudes of the signals into the base and emitter in an opposite direction and keeping the amplitude of the differential signal across the base and emitter constant (200 mV). The output of the detector varies between 143.3 mV and 145.6 mV. The maximum error is only 0.8%. The symmetric detector has completely symmetric structure and thus has less output variation than the nonsymmetric detector.

The differential circuit has the advantage of high rejection of common-mode noise. For a differential detector, it should also have the capacity to reject the common-mode noise which exists along with the differential signal being tested. The common-mode noise rejection characteristic is examined by adding an adjacent 5 GHz 20 mV harmonic as the common-mode noise on the base and emitter of the BJT in

the preceding detector transfer characteristics simulation. The transfer characteristics curve is identical to that without common-mode noise. So it further demonstrates the proposed differential detectors can not only measure the differential signal of interest but also reject the unwanted common-mode noise.

4.4 Experimental Results

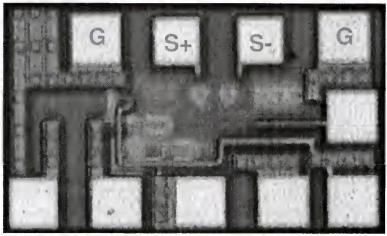
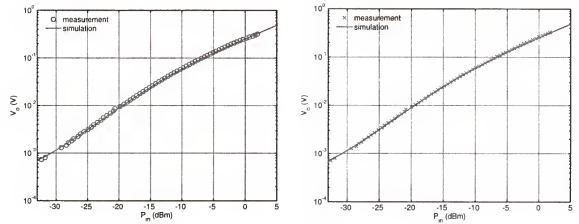


Figure 4–5: Chip photo of a nonsymmetric bipolar differential detector. (670×400 μm^2)

A nonsymmetric bipolar differential detector was fabricated using IBM 7WL BiCMOS process and is used in the six-port design in Chapter 6. The micrograph of the detector is shown in Figure 4–5. The chip size is 670×400 μm^2. The input and the reference bipolar transistors in the detector are both biased with 20 μA DC current. The resistors R_F is 5.1 kΩ and isolates the output capacitor from the BJT emitter.

Figure 4–6 is the detector's responses to a 5.2 GHz single-ended signal which is fed into the BJT base or emitter. The consistency of the measurement results with the simulation shows that the differential detector has an almost identical response no matter whether the signal is fed into the base or the emitter. Figure 4–7 is the



(a) (b)

Figure 4–6: The detector's responses to single-ended ac inputs (5.2 GHz) into (a) the base or (b) the emitter of the bipolar transistor.

detector's response to 5.2 GHz differential input signals. The measurement results are also consistent with the simulation. In this measurement, a single-ended ac signal is fed into an off-chip balun. Then the differential signal from the balun conveys onto the chip through a differential probe and is converted to DC output by the on-chip differential bipolar detector. The loss in the path from the balun input to the probe tip must be calibrated in order to obtain the transfer characteristics of the differential bipolar detector.

4.5 Conclusion

Nonsymmetric and symmetric differential detectors are proposed in this chapter. Both detectors have almost identical transfer characteristics as the Meyer power detector discussed in Chapter 2. The symmetric differential detector has a smaller ripple at the output and much shorter settling time than the nonsymmetric counterpart in Figure 4–2. However, the symmetric detector consumes more power and takes more area than the nonsymmetric counterpart. Both detectors have good high frequency

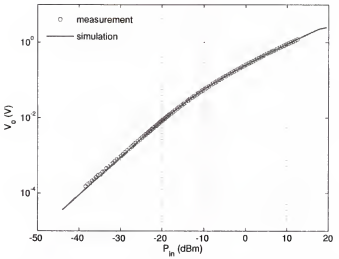


Figure 4–7: The detector's response to differential input ac signals (5.2 GHz).

response and high rejection to common-mode noise. A nonsymmetric differential detector is demonstrated and used later in the design of a six-port reflectometer for the measurement of the microwave reflection coefficients. As a promising circuit, the differential detector will have wide applications in embedded RFIC test.

CHAPTER 5
EMBEDDED SELF-TEST FOR LNA

5.1 Overview

With the development of the monolithic RF power detector, RF RMS detector and RF differential power detector, it becomes possible to probe the power level on the sensitive internal nodes of RF circuits. This chapter presents a new embedded self-test architecture that monitors the performance of a 5 GHz low noise amplifier such as transducer voltage gain, voltage gain, input impedance, etc. Moreover, a technique for the extraction of IIP3 from the input-output voltage gain transfer curve [42] can be employed with this test system.

A 5 GHz low noise amplifier with embedded self-test circuits was fabricated in 0.18 μm IBM 7WL process. The self-test architecture consumes about 15% additional die area and is easy to integrate with RF/microwave amplifiers. In this chapter, the integration of RF power detectors into a LNA design is presented, followed by algorithms for defining the criteria for the pass-and-fail parametric tests and experimental results for demonstration.

5.2 Embedded Self-Test Circuit

The block diagram of Figure 5–1 shows that two RF power detectors are inserted on the input and output ports of a 5 GHz low noise amplifier. These RF power detectors convert the probed RF signals to DC outputs, thus the sensitive LNA input and output RF nodes are monitored by measuring the DC voltages at the detector outputs. A RF signal source with an internal 50 Ω load is used at the input port and

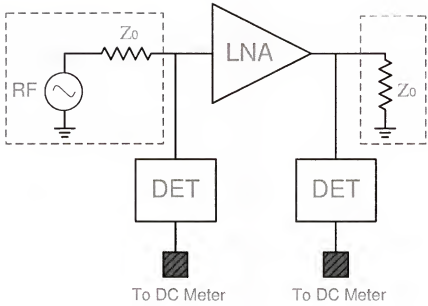


Figure 5–1: Block diagram of the embedded RF self-test circuit

another 50 Ω terminator at the output port. In this test set-up, the LNA works in normal operation and the added power detectors keep monitoring the performance of LNA without any interference. The Meyer power detector in Figure 2–1 has a very high input impedance and its input can be modeled as a small shunt capacitance which can be easily absorbed in the LNA matching network. So this detector has a negligible disturbance on the LNA performance and is selected for the built-in-self-test of the LNA. The transfer characteristic of the detector is calibrated by using a linearization technique [43]. The extraction algorithms in Section 5.4 provide the transducer voltage gain (G_T), voltage gain (G_V) and input matching of the low noise amplifier.

5.3 Integration of LNA and Detectors

A 5.2 GHz cascode LNA is designed and optimized for noise and gain. The LNA schematic diagram is shown in Figure 5–2. To integrate the detectors into the LNA matching circuits, the input of the detectors are modelled as small parasitic

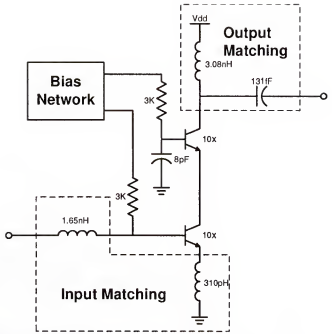


Figure 5–2: Schematic of cascode low noise amplifier.

capacitances (40 fF). The low noise amplifiers with embedded detectors was fabricated using IBM 7WL processes and the chip photo of the 5.2 GHz LNA with embedded detectors is shown in Figure 5–3. Most of chip area is taken by the on-chip inductors and bondpads. The detector size is very small but can be further reduced by using area-efficient sandwich capacitors or moving part of the capacitance off-chip. The measured result is shown in Section 5.5. This low noise amplifier is designed to have 19 dB transducer power gain and 1.6 dB noise figure at 5.2 GHz with 3 mA bias current.

5.4 Extraction Algorithms

This section presents the algorithms for the extraction of transducer voltage gain (G_T), voltage gain (G_V) and input impedance in the embedded RF amplifier test system. Then the corresponding criteria to separate faulty components from fault-free components can be defined with these extracted parameters.

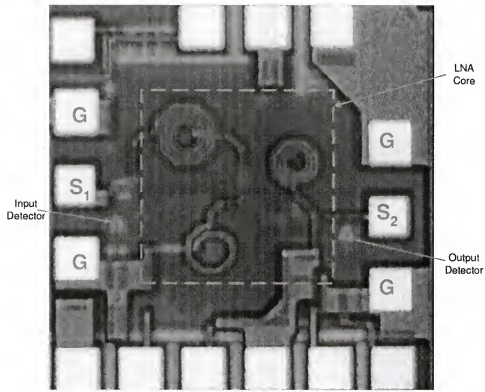


Figure 5–3: Chip photo ($760 \times 800 \mu m^2$) of 5.2 GHz LNA with embedded detectors using IBM 7WL process.

5.4.1 Transducer Voltage Gain (G_T) and Voltage Gain (G_V)

In the LNA measurement, the RF power detector at the input of the LNA gives a DC output V_{dc_i}. Then the input RF signal strength can be obtained by

$$V_{LNA_i} = G_i \cdot V_{dc_i} \tag{5.1}$$

where G_i is a constant that can be obtained from the transfer characteristics in Figure 2-6. Similarly, the output RF signal strength V_{LNA_o} can also be obtained by

$$V_{LNA_o} = G_o \cdot V_{dc_o} \tag{5.2}$$

where V_{dc_o} is the DC output of the RF power detector at the output of the LNA and G_o is a constant from Figure 2-6. Thus, the transducer voltage gain (G_{LNA_T}) and

voltage gain (G_{LNA_V}) are expressed respectively by

$$G_{LNA_T} = \frac{G_o \cdot V_{dc_o}}{V_{av_i}}$$
$$G_{LNA_V} = \frac{G_o \cdot V_{dc_o}}{G_i \cdot V_{dc_i}} \tag{5.3}$$

where V_{av_i} is, similar to the definition of available input power (P_{av_i}) [44], the available input ac signal amplitude when the input is matched perfectly.

The transducer voltage gain is equal to the parameter S_{21}, which is often defined in product's specification; the voltage gain is not defined in product's specification and can be obtained either from the transient simulation or from the calculation using

$$G_{LNA_V} = \left| \frac{S_{21}}{1 + S_{11}} \right| \tag{5.4}$$

(5.4) shows the difference between G_{LNA_T} and G_{LNA_V} is from the input matching condition. The voltage gain is approximately equal to the transducer voltage gain for a LNA with well-matched input. A large deviation between G_{LNA_V} and G_{LNA_T} occurs when the input matching is worse than -10 dB.

The transducer voltage gain and voltage gain in (5.3) are determined by the quality of the input matching, the output matching and the inner cascode amplifier status. The transducer voltage gain gives the information about output matching and inner amplifier status; the additional voltage gain provides the information about input matching if compared with transducer voltage gain. For example, a large deviation between the two gain curves indicates bad input matching. The transducer voltage gain and voltage gain are two important parameters and can be easily used to differentiate faulty components from fault-free components for production test. A specification on these two parameters can be defined and a low noise amplifier fails a

parametric test if the extracted transducer voltage gain and voltage gain from (5.3) are lower than their values in the specifications [45].

5.4.2 Input Impedance

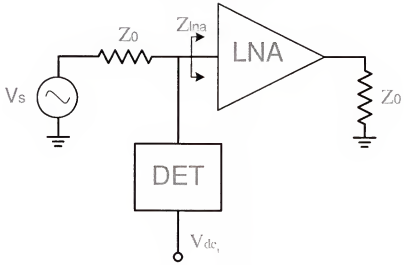


Figure 5–4: Block diagram from the signal source to the low noise amplifier.

The input impedance measurement [45] can be used to diagnose the defects at the input of a LNA. Usually for a good matching network, the real part of LNA input impedance $re(Z_{LNA_i})$ is approximate to 50 Ω and varies in the range of 50 ± 13 Ω due to process variation. The imaginary part of LNA input impedance is usually much smaller than its real part [45]. So, the input impedance can be represented only by its real part

$$|Z_{LNA_i}| = re(Z_{LNA_i}) \tag{5.5}$$

In the input impedance measurement, as seen in Figure 5–4, the signal source applies a constant signal V_s to the input of the LNA. The signal at the input of the LNA is

$$V_{LNA_i} = \frac{|Z_{LNA_i}|}{|Z_{LNA_i} + R_s|} \cdot V_s \tag{5.6}$$

Substitute (5.1) to (5.6) and let $R_s = 50\ \Omega$.

$$|Z_{LNA_i}| = \frac{50}{\frac{V_b}{G_i V_{dc_i}} - 1} \tag{5.7}$$

This equation is valid only for well-matched circuits. If the LNA has some catastrophic faults, the input impedance deviates from the value given by (5.7). So, the input impedance in (5.7) is another efficient means to differentiate faulty components from fault-free components for production test.

5.5 Experimental Results

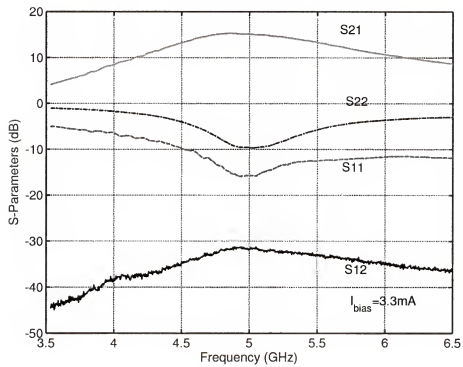


Figure 5–5: Measured S-parameters of a 5.2 GHz low noise amplifier.

A 5.2 GHz low noise amplifier was fabricated in 0.18 μm IBM 7WL process. Figure 5–3 is the chip photo of the LNA. It is seen that small power detectors are situated at the input and output connections near the bondpads. Figure 5–5 shows the measured S-parameters. The measured peak S_{21} is 15.4 dB at 5 GHz and its 3

dB bandwidth is 1.2 GHz from 4.4 GHz to 5.6 GHz. The measured S_{11} and S_{22} are -15.8 dB and -9.7 dB at 5 GHz, respectively. S_{21}, S_{11} and S_{22} are all tuned at 5 GHz, about 200 MHz deviation from the simulations. The measured S_{21} is about 4 dB less than the simulated S_{21}. Besides, some other measured parameters are $NF = 1.9$ dB and $P_{1dB} = -16$ dBm.

Though the fabricated LNA has degraded performance compared to the simulation, this LNA can be used for the demonstration of the built-in-self-test scheme in practical production test. Figure 5–6 shows the consistency between the transducer

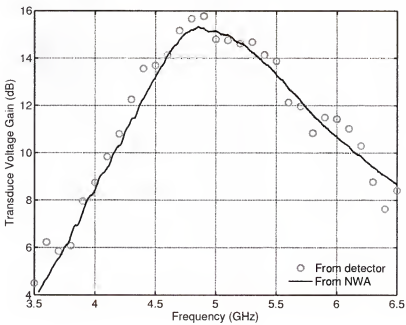


Figure 5–6: The measured S_{21} and extracted transducer voltage gain (G_{LNA_T}) of the low noise amplifier.

voltage gain (G_{LNA_T}) extracted respectively from the detector outputs and the measured S_{21} from the network analyzer. The input available ac signal amplitude V_{av_i} in (5.3) is obtained from the input ac power subtracting the loss in the cable and microwave probe.

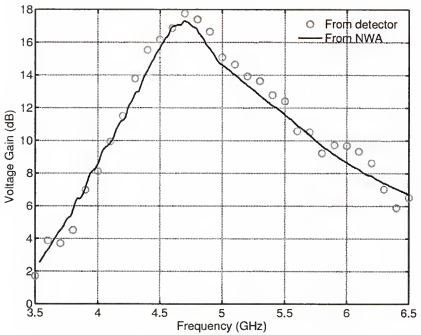


Figure 5–7: The measured LNA voltage gain from the respective NWA and detectors

.

Figure 5–7 shows the comparison of the measured voltage gain from the network analyzer and from the detectors. The measured voltage gain from the network analyzer is obtained from the simulation of the measured S-parameter data or the calculation using (5.4). It is seen that these two sets of measured voltage gain are consistent. The curve of the voltage gain is quite different from that of S_{21} in Figure 5–6. The voltage gain peaks at 4.7 GHz and has a narrower bandwidth than S_{21}. (5.4) shows that the difference of voltage gain and S_{21} is from the non-ideal input matching status S_{11}. Even though voltage gain is not the specification for a RF amplifier, voltage gain is very useful in the SOC design because the inherent voltage gain is the goal of design in an unmatched system.

The input impedance extracted from the detector is compared with that from the network analyzer in Figure 5–8. The consistency of two curves is seen for the

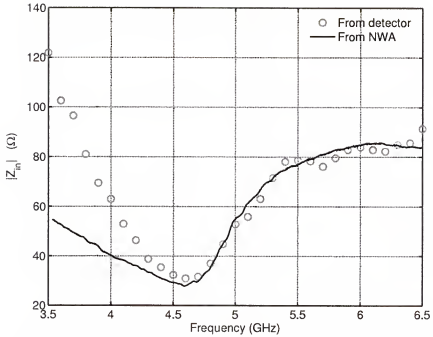


Figure 5–8: The measured LNA input impedance from the respective NWA and detectors.

frequencies above 4.5 GHz and there is a deviation between them for the frequencies below 4.3 GHz. The input impedance extraction method in Section 5.4 assumes the imaginary part of impedance is small and negligible. In Figure 5–9, the real part of the input impedance is large and the imaginary part is negligible at frequencies above 4.5 GHz. Thus the extracted impedance from the detector agrees with that from the network analyzer. However, at frequencies below 4.3 GHz, the real part of the input impedance is much less than the assumed lower bound resistance $-$ 37 Ω and the imaginary part is comparable to the real part. Thus the input impedance extraction method is no longer valid and a large deviation is seen in this frequency region. It is also seen in Figure 5–5 that this LNA has good matching with $S_{11} \geq$ -10 dB above 4.5 GHz where the two measured curves in Figure 5–8 agree. Moreover, the measured impedance in this frequency region can be used to derive the input

reflection coefficient. The input impedance extraction method is very effective in the production test, especially where the specification $S_{11} \geq$ -10 dB must be verified.

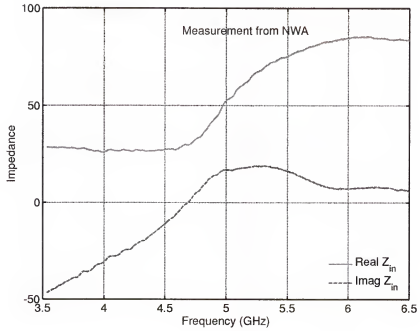


Figure 5–9: Comparison of real and imaginary part of the input impedance of the LNA.

5.6 Test Set-up

Chip-level RF measurements use microwave probes to conduct electrical signals between the DUT and the ATEs. The measurement results strongly depend on the probing condition. A good and a bad probing condition cannot be differentiated just using a microscope. ATE testers have an in-situ virtual display that facilitates the user to find and adjust a bad probing condition. However, in non-conventional measurement, to ensure or maintain a good probing condition is difficult. Our LNA testing needs to compare the measurement from the network analyzer and from the detectors. The LNA working condition and probing condition should be maintained identically during the operation of the two measurements. So the maintenance of the

LNA working condition and probing condition when switching the measurements is very important.

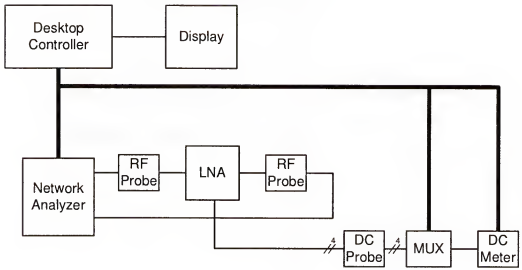


Figure 5–10: LNA test set-up.

Figure 5–10 shows the block diagram of the test set-up. The desktop controller communicates with the network analyzer, multiplexer and DC meter through the GPIB connections represented by the thick line in the figure. The network analyzer first measures the S parameters of the LNA, and then it is switched to be a RF signal source by the desktop controller. A RF signal is applied to the input of the LNA, and the outputs of the detectors are measured by the DC meter and stored in the desktop. In this test set-up, the switch of measurements is done inside the network analyzer and no change of cable connection is needed. Thus, identical LNA and probe working condition is maintained during the two measurements.

However, the port 2 of the network analyzer is used as the terminator at the output of the LNA and introduces some frequency-dependent variation at the detector outputs due to the long cable connection. Therefore, a 50 Ω terminator is used instead

at the output of the LNA and better consistency between the measurements from the detector and the network analyzer can be obtained. However, the change of the output connection of the LNA should be operated carefully to avoid any disturbance on the LNA working condition.

5.7 Conclusion

An embedded self-test system for the low noise amplifiers that uses two RF power detectors has been demonstrated with an additional die area cost of 15%. In the external equipment test set-up, only a RF signal generator, a 50 Ω terminator and several DC voltmeters are required. Compared to the conventional S-parameter measurement, this embedded self-test architecture is simple and cost-effective. This approach can measure the transducer voltage gain, voltage gain and input impedance, and is appropriate for the diagnosis of catastrophic faults and parametric faults in the production line.

CHAPTER 6
SIX-PORT REFLECTOMETER

6.1 Overview

Compared to measurements at low frequency, RF/microwave measurements represent a completely separate discipline. In the description of any RF/microwave systems or components, complex values are always used in the form of magnitude and phase. The scattering parameter (S-parameter) is often used in this scenario and it is represented by b_i/a_i where a_i, b_i are the complex amplitudes of incident and emergent power waves, respectively; i is the measurement port number.

RF power detectors can detect the peak or RMS amplitudes of signals but not their relevant phase information. So phase detectors are required to detect the phases. For the phase detection, the absolute amplitudes of signals must be known and large enough ($\geq$ 100 mV). For instance, the widely used phase and frequency detectors in the phase-lock-loop circuits (PLLs) are driven by digital signals. The phase detectors using Gilbert-cell circuits also need signals larger than 100 mV. The RF power detectors developed in the preceding chapters can detect the signal even below several milivolts. They have better sensitivity and may be used in the phase detection.

Phase detection can be realized just by using power detectors. Given the signals i and j are represented by

$$V_i = A\cos(\omega t + \phi_i) \tag{6.1}$$

$$V_j = B\cos(\omega t + \phi_j) \tag{6.2}$$

Thus, the difference of the two signals is

$$V = V_i - V_j = \sqrt{A^2 + B^2 - 2AB\cos(\phi_i - \phi_j)}cos(\omega t + \psi) \tag{6.3}$$

where, $\psi = \cos^{-1}(\frac{A\cos\phi_i + B\cos\phi_j}{\sqrt{A^2 + B^2 - 2AB\cos(\phi_i - \phi_j)}})$.
The amplitude of the signal difference V is determined by A, B and $\phi_i - \phi_j$ and can be measured by using a differential detector. The respective amplitudes of signals i and j (A and B) can be easily detected. Therefore, the phase information ($\phi_i - \phi_j$) can be reconstructed from these three amplitudes, and thus the measurement of S parameters can be realized just by using power detectors.

Back to 1970's, six-ports emerged as an alternative to conventional network analyzers. The conventional analyzers have the electronic complexity commensurate with the need to measure phase to high accuracy. In contrast, the six-ports are inherently simple and stable devices which do not need precision components but several power detectors. The theory of six-ports has been completed over several decades of development. The six-port reflectometer is widely explored to measure the reflection coefficient of a one-port device at high frequency [41, 46]. Besides, multi-port scattering parameter measurement systems have been developed on the basis of one or more six-port reflectometers. For embedded RF/microwave IC test, the six-ports attract more attention because of the simplicity and monlithic integration capability. An area-efficient monolithic six-port reflectometer consisting of resistive power divider, phase shifter and diode power detectors was developed using a GaAs process and it operates between 1.3 GHz and 3.0 GHz [41]. Thanks to the development of bipolar power detectors, this six-port reflectometer and/or other similar monolithic integrated circuits can be migrated to the popular SiGe technology. This chapter is

organized as the following: Section 6.2 and Section 6.3 review the theory of six-port reflectometer and related calibration techniques; Section 6.4 and Section 6.5 present the design of a six-port reflectometer for embedded RF IC test and some measurement results. Besides, Appendices B and C introduce the fundamentals of two-port networks and impedance measurement which is helpful for the understanding of the six-port theory.

6.2 Theory of Six-Port Reflectometer

As an alternative to conventional network analyzers, the six-port techniques including reflectometers, multiport network analyzers, etc have been developed over several decades. The theory of six-port reflectometer is the basis of the six-port techniques and is presented in this section.

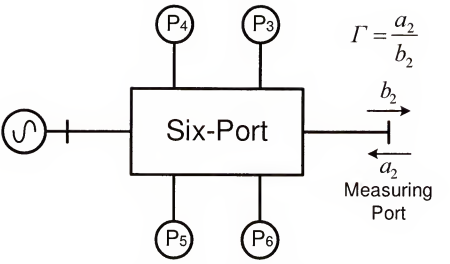


Figure 6–1: Block diagram of a six-port reflectometer.

As seen in Figure 6–1, the test signal is fed from an RF signal source to the input port (port 1) of a six-port structure. The output measuring port (port 2) is connected with the device under test (DUT). The reflection coefficient Γ at the measuring port is the measurand of interest. In this configuration, four power detectors are placed

on the elaborate-designed four ports for the extraction of reflection coefficient Γ since Γ can not be obtained directly.

Assuming that the six-port structure is linear, but otherwise arbitrary, it has been shown [47, 48] that the power levels given by the power detectors can be expressed respectively by

$$P_3 = |Aa_2 + Bb_2|^2 \tag{6.4}$$

$$P_4 = |Ca_2 + Db_2|^2 \tag{6.5}$$

$$P_5 = |Ea_2 + Fb_2|^2 \tag{6.6}$$

$$P_6 = |Ga_2 + Hb_2|^2 \tag{6.7}$$

where a_2, b_2 are the waves proceeding left and right, respectively through the measuring port in Figure 6–1; $A \sim H$ are the complex constants whose values are determined primarily by the six-port structure. These values can be obtained in the characterization of six-port structure.

It has been shown in [49,50] that one solution to (6.4)$\sim$(6.7) is given by

$$|b_2|^2 = \sum_{i=3}^{6} \beta_i P_i \tag{6.8}$$

and

$$\Gamma = \frac{\sum_{i=3}^{6} (C_i + jS_i) P_i}{\sum_{i=3}^{6} \beta_i P_i} \tag{6.9}$$

where C_i, S_i and β_i are real and functions of $A \sim H$. In the derivation of this solution, however, the fact that the system is overdetermined (i.e., only three detectors are required) was ignored. Moreover, this approach yields little insight into how to choose $A \sim H$ so as to best exploit the method. Except for the design criteria which may emerge from the study of (6.4)$\sim$(6.7), there is the additional practical requirement

of correcting for power instability in the signal source and ensuring that the power levels at the several detectors and output port are maintained at some optimum value as the frequency varies [48]. Thus, a detector is used to measure the incident wave amplitude $|b_2|$ with the aid of a directional coupler or other devices. Here, the port 3 is chosen for this role and, therefore, $A = 0$ is the design objective. When the condition is realized, (6.4) becomes

$$P_3 = |B|^2|b_2|^2 \tag{6.10}$$

rewrite (6.5), (6.6) and (6.7) with respect to b_2 and Γ as

$$P_4 = |C|^2|b_2|^2|\Gamma - q_4|^2 \tag{6.11}$$

$$P_5 = |E|^2|b_2|^2|\Gamma - q_5|^2 \tag{6.12}$$

$$P_6 = |G|^2|b_2|^2|\Gamma - q_6|^2 \tag{6.13}$$

where $q_4 = -D/C, q_5 = -F/E$ and $q_6 = -H/G$.

Then, (6.11), (6.12) and (6.13) are divided by (6.10) to eliminate the term $|b_2|^2$. Thus, we have, for example,

$$|\Gamma - q_4|^2 = \left|\frac{B}{C}\right|^2 \cdot \frac{P_4}{P_3} \tag{6.14}$$

P_3, P_4 are the measured results from the power detectors. $|B/C|^2$ and q_4 are known from the characteristics of the six-port structure. Thus, (6.14) represents a circle with center at q_4 on the Γ plane as shown in Figure 6–2. The radius of the circle is already determined to be $\left|\frac{B}{C}\right| \sqrt{\frac{P_4}{P_3}}$ from (6.14). The Γ value is inside the unit circuit if the measured termination is passive. Similarly, a circle with center at q_5 and a

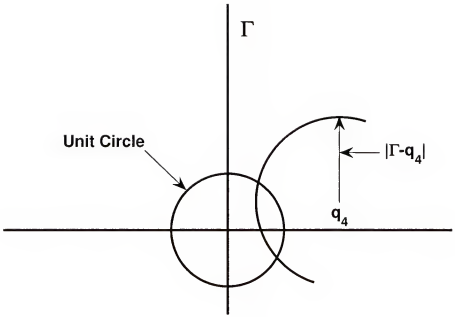


Figure 6–2: Γ circle determined by P_3 and P_4.

circle with center at q_6 can also be obtained. The intersection of those three circles gives the wanted reflection coefficient Γ.

As a matter of fact, sometimes, the reflection coefficient Γ can be obtained directly from two circles when one intersection point is inside the unit circle and one outside of the unit circle as shown in Figure 6–3. This is so-called five-port technique which does not need an additional P_6 detector. However, in some cases, the two intersection points both fall inside the unit circle and give two values for Γ. Therefore, P_6 detector is needed to determine the correct Γ. Moreover, this redundant detector can improve the accuracy. As shown in Figure 6–4, the three circles centered in q_4, q_5 and q_6 on the Γ plane ideally intersect in a point. However, due to the errors in the practical measurement, the three circles may not intersect in one point and thus some statistics weighting must be used to find the optimum Γ. Intuitively, the additional detector P_6 improves the accuracy in Γ determination. This improvement is apparent

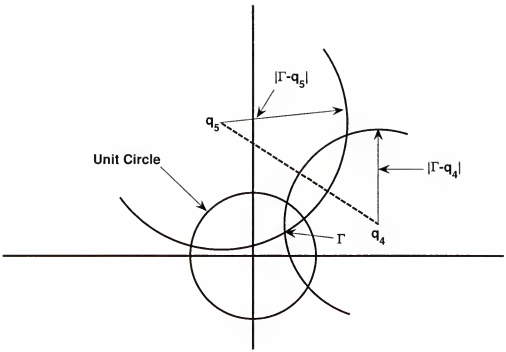


Figure 6–3: Determination of Γ from the intersection of two circles.

when the circle of detector P_4 is closely tangent to that of detector P_5. In this case, the position of Γ is in a direction perpendicular to the line between q_4 and q_5 and is sensitive to errors in P_4 and P_5. One more circle of detector P_6 helps to determine Γ value and reduces the sensitivity to errors. Moreover, it solves the problem of double root ambiguity in five-port technique.

The design criteria for six-port technique [46, 48] is $|q_4| = |q_5| = |q_6| = |q|$ while the three points q_4, q_5 and q_6 differ by $\pm 120°$. The optimum choice of $|q|$ is expected to lie in the range of $0.5 \sim 1.5$.

6.3 Six-Port Calibration

The theory of six-ports is complete so that, at least in principle, they can return highly precise results if a proper calibration procedure is implemented. Many methods have been proposed for the calibration of six-ports [48]. Among them, the six- to

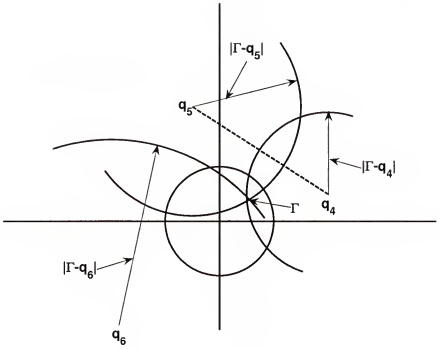


Figure 6–4: Determination of Γ from the intersection of three circles.

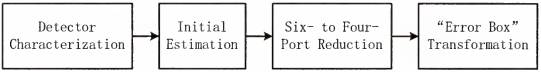


Figure 6–5: Calibration of the six-port reflectometer.

four-port reduction technique proposed by Engen [51] is more attractive and widely accepted as the basis for six-port calibration.

The popular calibration procedures for six-port reflectometer are shown in Figure 6–5. First, the off-line or in-situ characterization is employed to find the characteristics of power detectors used in the six-port. Then, the initial values of w_1, w_2, Z and R for the six- to four-port reduction are estimated. Next, the six- to four-port reduction procedure is to find the optimum values for the parameters in W plane. Finally, some well-defined standards are measured to find the coefficients in the bilinear

"error box" transformation between the Γ plane and the W plane. The calibration procedures are presented in detail in Appendix D.

6.4 Six-Port Implementation

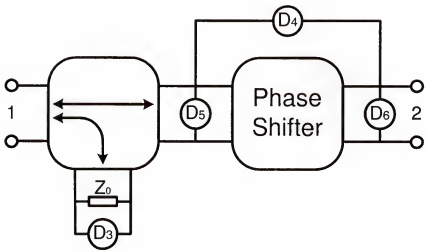


Figure 6–6: Block diagram of the on-chip six-port reflectometer.

The design criteria for a six-port is $|q_4| = |q_5| = |q_6| \in [0.5, 1.5]$ and the phases of the points q_4, q_5 and q_6 differ by $\pm 120°$. For on-chip implementation, these q points can be realized using a simple low-pass phase shifter. An on-chip six-port reflectometer was developed in [41] and its block diagram is shown in Figure 6–6. The six-port structure is a power divider which leads a part of incident power from the source at port 1 to the matched reference power detector D_3 at port 3, followed by a phase shifter which is surrounded by three power detectors D_4, D_5 and D_6 with high input impedance.

Assuming in an ideal case that the power divider has no power loss and the power detector has infinite input impedance, the coefficients A_i and B_i of the structure are

the function of the phase shift ϕ produced by the phase shifter. These coefficients are

$$\begin{aligned} A_4 &= e^{-j\phi} - 1 \\ A_5 &= e^{-j\phi} \\ A_6 &= 1 \\ B_4 &= e^{j\phi} - 1 \\ B_5 &= e^{j\phi} \\ B_6 &= 1 \end{aligned} \tag{6.15}$$

Using $q_i = -\frac{B_i}{A_i}$, the points q_i are given

$$\begin{aligned} q_4 &= e^{j\phi} \\ q_5 &= -e^{j2\phi} \\ q_6 &= -1 \end{aligned} \tag{6.16}$$

The three points q_4, q_5 and q_6 have the same unit amplitude but different phases. Their phases are $\phi, 180° + 2\phi$ and 180°, respectively. The optimum ϕ is set to 60° so as to achieve the 120° phase difference among the points q_4, q_5 and q_6. In fact, six-port technique allows the phase difference between the points q_i to be at least 40°. Thus, the value of ψ can be in the range of 20° to 140°. Figure 6–7 shows the determination of the reflection coefficient Γ from the three circles using this six-port technique. The locus of the points q_i are $1/2 \pm j\sqrt{3}/2$, and -1.

The six-port reflectometer in Figure 6–6 consists of a power divider, a phase shifter and several power detectors. The power divider as shown in Figure 6–8 has a resistive structure similar to a Wheatstone bridge. The resistive power divider not only has an ideally unlimited bandwidth but also takes much smaller chip area than that of the reactive counterpart. So it is preferred for embedded RFIC test. In Figure

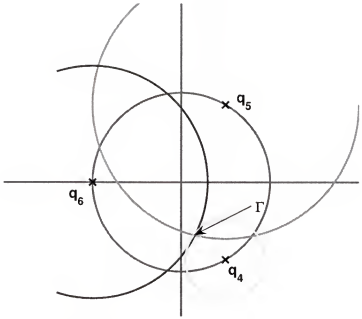


Figure 6–7: Determination of Γ from the three circles with centers at $1/2 \pm j\sqrt{3}/2$, and -1.

6–8, when $R_1 R_2 = R_0^2$, the scattering matrix S of the power divider with respect to R_0 is given by

$$S = \begin{bmatrix} 0 & \frac{1}{1+\frac{R_1}{R_0}} & \frac{1}{1+\frac{R_2}{R_0}} \\ \frac{1}{1+\frac{R_1}{R_0}} & 0 & 0 \\ \frac{1}{1+\frac{R_2}{R_0}} & 0 & 0 \end{bmatrix} \tag{6.17}$$

It is seen from (6.17) that all three ports are matched and port 2 and 3 are isolated from each other. In our design, the resistances of R_0, R_1 and R_2 are all 50 Ω to achieve an equal power splitting. Thus the power divider has 6 dB attenuation on each branch, which is 3 dB more than that of the lossless power divider. For on-chip implementation, the parasitic capacitance of resistors may degrade the frequency response of the power divider. IBM 7WL BiCMOS process has $K1$-type resistor with very small parasitic capacitance and the power divider designed with this kind of resistor has a flat frequency response even over 20 GHz. Thus, this power divider can

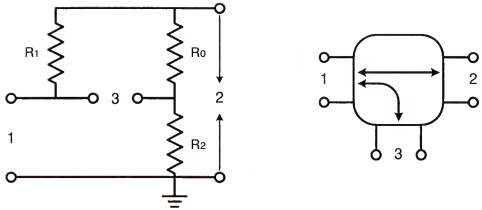


Figure 6–8: Schematic of the resistive power divider.

be treated as a frequency independent component in the objective frequency range (up to 7 GHz).

Figure 6–9 is the $T-$type phase shifter which consists of two series inductors and one capacitor shunt to ground. This phase shifter is low-pass with 50 Ω characteristics impedance and it is designed to have 60° phase shift around the operating frequency – 5 GHz. The phase of this structure decreases at a rate of about 16.3°/GHz. Thus, the six-port reflectometer using this phase shifter may have 7 GHz bandwidth in which the phase difference between the points q_i is at least 40°.

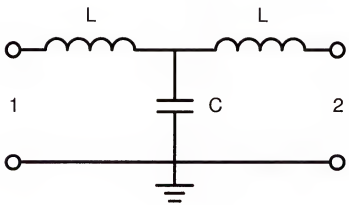


Figure 6–9: Schematic of the phase shifter.

The six-port reflectometer has four detectors $D_3 \sim D_6$ as shown in Figure 6–6 and one reference detector. The detectors D_3, D_5 and D_6 are the single-ended Meyer power detector in Figure 2–1 and D_4 is the differential bipolar power detector in Figure 4–2. They all have the merit of high input impedance. The operation principles of these detectors are presented in Chapter 2 and Chapter 4. All the detectors are biased with an external voltage source to circumvent any noise effect.

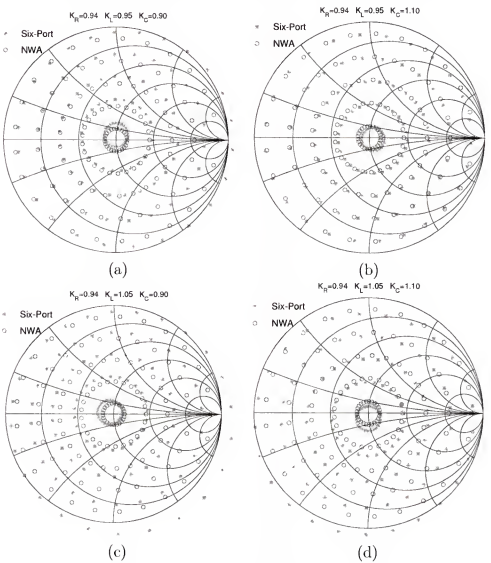


Figure 6–10: The deviation of reflection coefficient from the corner analysis of the six-port reflectometer ($K_R = 0.94$).

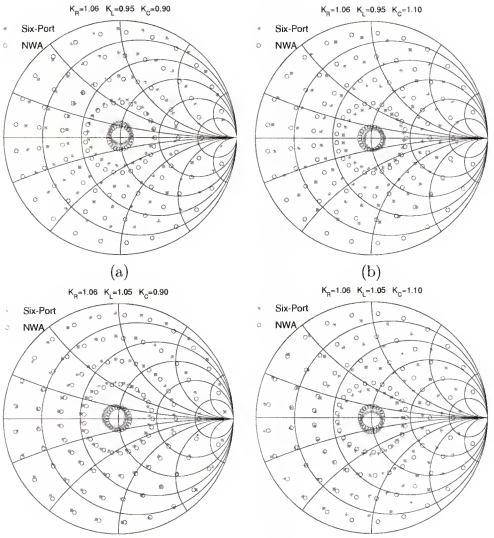


Figure 6–11: The deviation of reflection coefficient from the corner analysis of the six-port reflectometer ($K_R = 1.06$).

The tolerance to process variation is studied to verify if the six-port reflectometer is appropriate for embedded test. Besides the detectors, the resistors, inductors and capacitors in the power divider and phase shifter have certain amount of variation and affect the performance of the reflectometer in different ways. The variation in these components may cause a reduced directivity of power divider, and change the phase shift and characteristic impedance of the phase shifter. However, these

changes have weak influence on the characteristics of the reflectomer. Figure 6–10 and Figure 6–11 is the variation of the reflectometer performance in the worst-case simulation, assuming the resistor, inductor and capacitor varies respectively within 6% (from IBM 7WL), 5% and 10% (from IBM 7WL) and the detector has negligible variation. The five circles on Smith chart from the network analyzer are the constant Γ-circles with $|\Gamma|$ =(0.1, 0.3, 0.5, 0.7, 0.9) from the inside to outside; the other five circles are derived from the response of the six-port in the worse-case conditions, using the calibrated six-port parameters (nominal values). K_R, K_L and K_C are the respective ratios of real component values to nominal values for the resistor, inductor and capacitor. The Γ-circle from the six-port reflectometer when $K_L = 0.95$, $K_C = 0.90$ deviates in a direction opposite to that when $K_L = 1.05$, $K_C = 1.10$. Similarly, the Γ-circles for $K_L = 0.95$, $K_C = 1.10$ and $K_L = 1.05$, $K_C = 0.90$ also deviate in an opposite direction. The maximum Γ deviation values ($|\Gamma_{SPR} - \Gamma_{NWA}|$ and $|\Gamma_{SPR}| - |\Gamma_{NWA}|$) for the circles in Figure 6–10 and Figure 6–11 are listed in Table 6–1. The deviation $|\Gamma_{SPR} - \Gamma_{NWA}|$ increases from the inside to outside. The inner-most circle ($\Gamma = 0.1 = -20$ dB) corresponds to the well-matched area. The second inner-most circle has the reflection around -10 dB and the worst reflection deviation $\Delta|\Gamma|$ up to 2 dB. The remaining circles also have up to 2 dB reflection deviation. The area outside the second inner-most circle is of the interest for production test, because this area is usually where the specification is defined. From the above analysis, the six-port reflectometer can be integrated with the DUT and measure the reflection coefficient of the DUT with up to 2 dB deviation without any costly calibration. Thus, the on-chip six-port reflectometer, as an alternative test

solution, may be used to diagnose parametric and catastrophic faults in production test.

Table 6–1: The maximum deviation of reflection coefficients from the corner analysis of the six-port reflectometer. ($|\Delta\Gamma| = |\Gamma_{SPR} - \Gamma_{NWA}|$, $\Delta|\Gamma| = |\Gamma_{SPR}| - |\Gamma_{NWA}|$)

Corners	$\Gamma = 0.1$	$\Gamma = 0.3$	$\Gamma = 0.5$	$\Gamma = 0.7$	$\Gamma = 0.9$
(K_R, K_L, K_C)	$\lvert\Delta\Gamma\rvert$, $\Delta\lvert\Gamma\rvert$(dB)	$\lvert\Delta\Gamma\rvert$, $\Delta\lvert\Gamma\rvert$(dB)	$\lvert\Delta\Gamma\rvert$, $\Delta\lvert\Gamma\rvert$(dB)	$\lvert\Delta\Gamma\rvert$, $\Delta\lvert\Gamma\rvert$(dB)	$\lvert\Delta\Gamma\rvert$, $\Delta\lvert\Gamma\rvert$(dB)
0.94,0.95,0.90	0.056,4.23	0.083,1.54	0.117,1.15	0.162,1.14	0.218,1.28
0.94,0.95,1.10	0.039,3.88	0.048,1.01	0.060,0.45	0.075,0.19	0.093,0.19
0.94,1.05,0.90	0.052,3.62	0.066,1.66	0.083,1.26	0.146,1.65	0.240,2.05
0.94,1.05,1.10	0.060,4.79	0.084,1.89	0.110,1.52	0.139,1.43	0.173,1.43
1.06,0.95,0.90	0.050,5.28	0.072,1.98	0.097,1.54	0.123,1.44	0.153,1.44
1.06,0.95,1.10	0.043,4.90	0.060,1.86	0.079,1.38	0.127,1.72	0.190,2.06
1.06,1.05,0.90	0.041,3.88	0.049,0.92	0.060,0.43	0.074,0.21	0.091,0.28
1.06,1.05,1.10	0.054,5.76	0.080,1.92	0.114,1.36	0.155,1.31	0.204,1.45

6.5 Test Set-up and Measurement Results

A six-port reflectometer was fabricated using 0.18 μm IBM 7WL technology. Figure 6–12 shows the chip photo of the six-port reflectometer. The six-port core size is only 400×350 μm^2 and the chip core area contains a phase shifter, a power divider and several detectors. Most of the chip area is occupied by the bondpads and the low-pass capacitors. Some alternations such as using composite capacitors can be done to minimize this scattering parameter detector for the embedded RFIC test.

The six-port reflectometer is calibrated in the procedures presented in Section D. First, the detectors are linearized at 5 GHz using the method in [43]. The order of the linearization is 7 and the number of measured loads is 5 to 7. This method can characterize a detector in-situ without the need of a reference power meter or a repeatable attenuation step. Then, the initial estimates are found using the method proposed by Stumper [52]. Six equally-distributed sliding shorts are used as loads

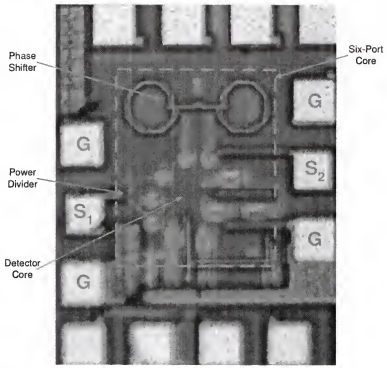


Figure 6–12: Chip photo of the six-port reflectometer.

for calibration. However, it is hard to achieve a truly sliding short in our test set-up because the connected cable and probe introduce about 0.2 dB loss at 5 GHz. Therefore, some modification on the algorithm of finding initial estimates is made correspondingly for this specific measurement. Next, Engen's six- to four-port reduction technique is used and lastly, the virtual four-port is achieved by using three known loads (open, short and 50 Ω load) just like SOL calibration for conventional network analyzer.

The measurement set-up is shown in Figure 6–13. This set-up consists of a desktop controller, a network analyzer (also used as an ac signal source), a probe station, probe heads, a multiplexer, a DC meter and some DC supplies. The desktop controller communicates with the network analyzer, multiplexer and DC meter via GPIB cables. The GPIB cable connections are represented by the thick line in Figure

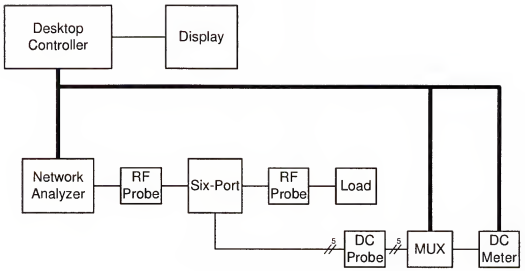


Figure 6–13: The test set-up for six-port reflectometer.

6–13. Unlike some commercial automatic test equipments for six-ports, this set-up is semi-automatic because the sliding short is tuned manually. The quality of the measurement may be degraded since the mechanical tuning is opt to disturb the system under test.

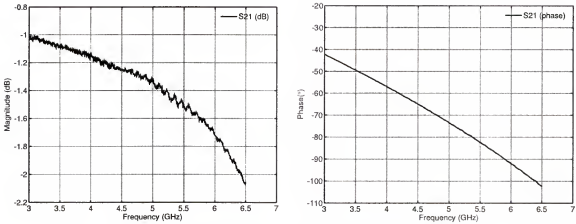


Figure 6–14: Measured S_{21} of the phase shifter

The measured S_{21} in Figure 6–14 shows the phase shifter has 72° phase shift and 1.3 dB loss at 5 GHz. The measured phase decreases at a rate about 16.5°/GHz and it

is consistent with the simulation including the parasitic of the interconnect. However, the measured loss is about 0.7 dB more than the simulation. This is due to the skin effect and the frequency-dependent loss of the low-pass phase shifter. Figure 6–15 shows the measured attenuation from port 1 to port 2 of the six-port reflectometer increases from 7.3 dB at 3.5 GHz to 9.5 dB at 6.5 GHz due to the low-pass character of the phase shifter. According to the above measured phase shift and attenuation results, the six-port reflectometer may have a bandwidth at least from 3.5 GHz to 6.5 GHz if a deliberated calibration is applied to.

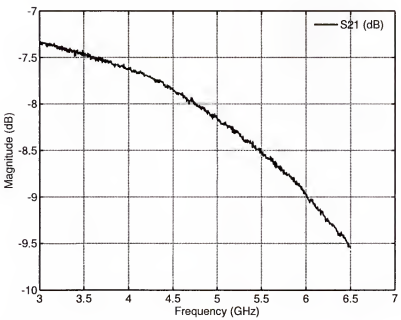


Figure 6–15: Measured $|S_{21}|$ of the six-port reflectometer

The calibration of the six-port reflectometer gives the centers of the three circles in the W plane, thus their corresponding q-points can be derived using the bilinear "error box" transformation. Figure 6–16 is the measured absolute values of the q-points. These absolute values of q_4 and q_5 are between 1.2 and 2.8 while that of q_6 varies in a narrow range between 1.2 and 1.8. Due to the attenuation of the path

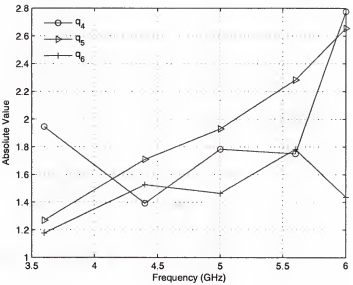


Figure 6–16: Measured absolute values of the q-points.

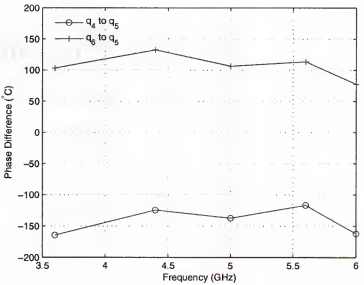


Figure 6–17: Measured phase differences between the q-points.

from the power detectors to the output bandpad at port 2, all the absolute values of $q-$points are larger than the ideal value 1.0. As the frequency increases, the absolute values of q_4 and q_5 increase. It shows that the path losses from detector D_4 and detector D_5 to the output increase with frequency. These losses are mainly due to the frequency dependent character of the low-pass phase shifter and the lossy substrate. Figure 6–17 is the measured phase differences between the $q-$points. It shows the optimum frequency range with phase differences around 120° is between 4 GHz and 5.6 GHz. As frequency goes above 6 GHz, the phase differences deviate far from 120° and the converge problem may come out. Advanced calibration technique [53] may help to improve the quality of measurement.

The reflection coefficients Γ_{SPR} measured with the six-port reflectometer are compared with the reflection coefficients Γ_{NWA} measured with a commercial network analyzer. The measured results at 5 GHz in Figure 6–18 shows the two sets of reflection coefficients match very well. The maximum absolute value $|\Gamma_{SPR} - \Gamma_{NWA}|$ is 0.05 and the maximum phase difference $\angle(\frac{\Gamma_{SPR}}{\Gamma_{NWA}})$ is 5° for the load distributed on the Smith chart with $|\Gamma| < 0.6$.

As a compact impedance measurement device, this six-port reflectometer has enough precision for embedded RF IC test. It can precisely measure the impedance mismatch with Γ below -6 dB. This coverage is large enough to test impedance variation at internal nodes and diagnose the malfunctions in the DUT. The six-port reflctometer may have full coverage over the whole smith chart if some improvements are made in the calibration. Some difficulties exist in the current measurement. First, the manual-tunable sliding short is not as repeatable as expected. It may introduce $4 \sim 5°$ phase variation at some sliding positions. Second, the manual tuning of sliding

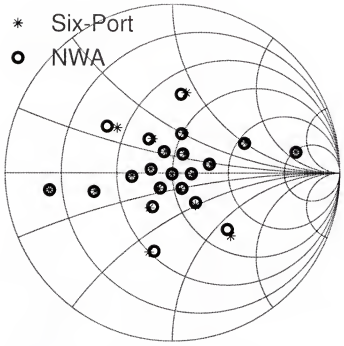


Figure 6–18: Comparison of Γ from the six-port reflectometer and commercial network analyzer.

short may disturb the measurement system, which could ruin the whole calibration. Third, the path between the output port 2 and the sliding short has some loss and the $|\Gamma|$ of the load seen at the port 2 is about 0.75, not 1 as suggested by Stumper [52]. Some other calibration methods [53] may improve the quality of the parameter estimates in the six- to four-port reduction and efficiently eliminate some cases which is "ill-conditioned" in Stumper's method.

6.6 Conclusion

An on-chip six-port reflectometer using bipolar RF detectors is developed using a BiCMOS process. The reflectometer has a simple structure including a power divider, a phase shifter and several bipolar RF detectors. The core chip size is small and the circuit is easily embedded for RF testing. A description of the calibration method

is presented. The calibration includes four procedures – detector characterization, initial estimation, six- to four-port reduction and "error box" transformation. With this calibration method, the six-port reflectometer achieves high measurement precision which is comparable to the commercial network analyzer. Advanced calibration and measurement set-up may improve the six-port measurement accuracy and bandwidth. This on-chip reflectometer is tolerant to process variation and is very suitable for embedded RF IC testing.

CHAPTER 7
FUTURE CALIBRATION-FREE DETECTORS

7.1 Overview

Any measuring device must be set or corrected before usage, usually by adjusting it to match or conform to a dependably known and unvarying measure. This procedure – calibration is very tedious and time-consuming, especially in RF/microwave testing. For example, a network analyzer must be calibrated using some well-known standards (calkit) before the measurement; a microwave power meter using a 50 MHz signal source.

Calibration is usually required in embedded test due to process variation, mismatch, etc. Embedded test circuits with self-calibration capability were reported in the literature [6]. However, the calibration results in higher cost of testing and higher design complexity, and even worse, it may become impossible in some cases such as embedded RF IC testing. The well-defined standards for calibration in RF testing cannot be implemented on-chip, and thus embedded test circuits can not be self-calibrated. Replica test method has ever been used for solving the calibration problem. A replica test circuit is placed on-chip in a near place beside the test circuit which is integrated for testing the circuit under test (CUT). This replica test circuit can be characterized individually, assuming it has the same characteristics as the one for testing the CUT. The additional chip headroom and calibration prohibit the

population of this method. This chapter introduces the calibration-free design concept for embedded RF testing, analyzes the variation in the detectors and proposes a calibration-free detector design for practical application.

7.2 Error Analysis

The analysis of Meyer power detector in Figure 2–1 in Chapter 2 assumes the Meyer power detector has identical bipolar transistors (Q_1, Q_2), current sources (I_1, I_2), and bias resistors (R_1, R_2). However, in the practical application to embedded RF IC testing, this assumption may not be valid.

The transistors Q_1 and Q_2 have large mismatch because their size is minimized for processing high-frequency signals. This mismatch is mainly from the difference of the saturation current I_S of bipolar transistors. As in Chapter 2, the mismatch in the Meyer power detector is analyzed in the large-signal linear region and the small-signal square-law region.

Assuming the saturation current of Q_1 (I_{S1}) is κ times that of Q_2 (I_{S2}). In large-signal linear region, (2.4) is rewritten as

$$I_{S1}e^{\frac{V_{BE1}}{V_T}}\frac{e^{\frac{V_{ac}}{V_T}}}{\sqrt{2\pi V_{ac}/V_T}} = I_{S2}e^{\frac{V_{BE2}}{V_T}} \tag{7.1}$$

The bases of Q_1 and Q_2 are voltage-biased identically. Therefore, the output voltage (V_o) is related to ac input-signal amplitude (V_{ac}) by

$$V_o = V_{ac} - V_T \ln \sqrt{2\pi V_{ac}/V_T} + V_T \ln \kappa \tag{7.2}$$

The mismatch of the bipolar transistors introduces a DC offset $V_T \ln \kappa$. 20% mismatch in I_S leads to 4.8 mV offset at room temperature. This error is not significant in the large-signal linear region since the output is large.

In small-signal square-law region, (2.7) is rewritten as

$$I_{S1}e^{\frac{V_{BE1}}{V_T}} \cdot (1 + \frac{V_{ac}^2}{4V_T^2}) = I_{S2}e^{\frac{V_{BE2}}{V_T}} \tag{7.3}$$

Using $\ln(1+x) \simeq x$, the output voltage (V_o) is expressed by

$$V_o = V_T \cdot \ln(1 + \frac{V_{ac}^2}{4V_T^2}) + V_T \ln \kappa \simeq \frac{V_{ac}^2}{4V_T} + V_T \ln \kappa \tag{7.4}$$

The mismatch of the bipolar transistors also introduces a DC offset $V_T \ln \kappa$. However, this error from the offset is significant in the small-signal square-law region and calibration is needed before the measurement. (7.2) and (7.4) shows the whole transfer curve shifts by the DC offset $V_T \ln \kappa$. This DC offset voltage can be obtained in a DC measurement without applying any ac signal. Therefore, the detector output subtracting the DC offset in DC measurement becomes independent of the process variation and mismatch. Figure 7–1 is the Monte-Carlo simulation results (1000 simulations) in various conditions, assuming identical bias currents and bias resistors. Figure 7–1.(a), 7–1.(c), and 7–1.(e) are simulated with a 200 mV 5.2 GHz sinusoidal signal. Figure 7–1.(a) and Figure 7–1.(c), are the distribution of the output voltage V_o simulated respectively with process variation only and process variation plus mismatch. They show very small variation of V_o, demonstrating their process-independent merit in the large-signal detection region. Figure 7–1.(b), 7–1.(d) and 7–1.(f) are simulated with a 20 mV 5.2 GHz sinusoidal signal. Figure 7–1.(b) simulated with process variation shows 0.18% variation of output voltage V_o. However, Figure 7–1.(d) simulated with process variation plus mismatch shows 16.7% output variation, and therefore, calibration is definitely necessary in small-signal detection region. Figure 7–1.(e) and Figure 7–1.(f) are the distribution of the output voltage

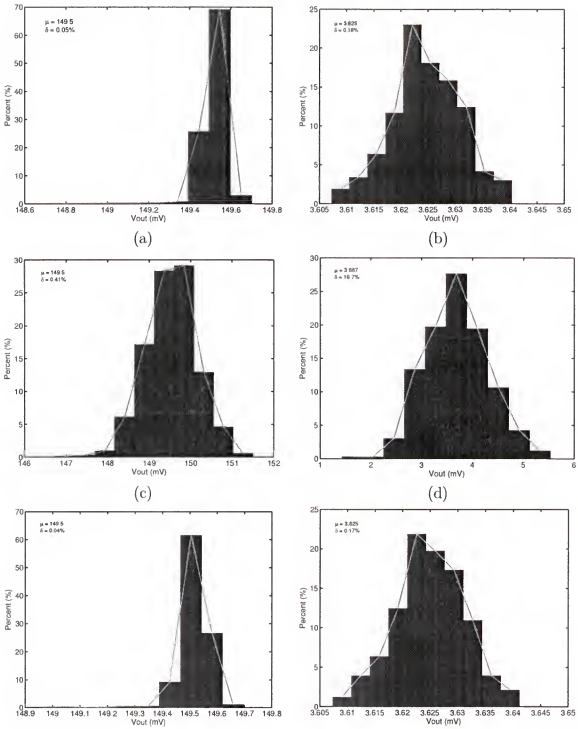


Figure 7–1: Output distribution from different Monte Carlo simulation (a, c, e) with 200 mV and (b, d, f) with 20 mV 5.2 GHz sinusoidal signals. (sample size 1000, room temperature)

after subtracting the DC offset in DC measurement respectively in the large-signal and the small-signal detection region. Both shows very small variation. The variation in small-signal detection region decreases from 16.7% before DC calibration to 0.17% after the DC calibration.

Other sources of errors are from the mismatch of bias resistors and bias current sources, power supply, ground and substrate noise. The noise in power supply, ground and substrate may change the output by affecting the bias current sources. The errors from the mismatch of bias resistors and bias current sources can be canceled in DC calibration, but not for power supply noise and ground noise due to the time-varying character. Thus, careful design in the bias current source is important.

7.3 Single-Transistor Detector

The requirement of DC calibration for canceling the offset voltage due to the mismatch in Meyer power detector counteracts the advantages of the inherent differential structure such as common-mode rejections. Therefore, a single-transistor detector is more appropriate for embedded RF IC test and is proposed as the substitute of Meyer power detector.

The single-transistor detector is shown in Figure 7–2. The bipolar transistor, bias resistor and low-pass capacitor are on-chip; the current sources may be on-chip or off-chip. If the current sources are from off-chip, the total bondpads of the detector except for power supply and ground are only two, relieving the pressure of chip headroom. The switch on the left current source is on in temperature measurement and off in normal detection. The detector output is measured, respectively, with and without applied ac signals within a short time. The difference of the measured voltages is the wanted output value used to estimate the applied ac signal strength.

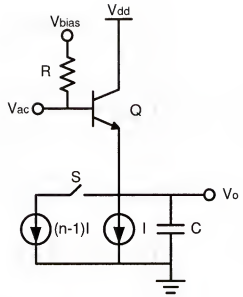


Figure 7–2: Schematic of a single-transistor power detector.

Assuming the bias current and the temperature of the chip are constant over the time, the output values for large-signal detection region and small-signal detection region are represented respectively by (2.5) and (2.8) and thus are independent of process variation. The single-transistor detector is easy for design and has less loss from the interconnects than Meyer power detector with complicated routing for common centroid layout.

(2.8) contains a temperature-related parameter – thermal voltage ($V_T = \frac{KT}{q}$). V_T is about 25.9 mV at room temperature and linearly proportional to absolute temperature T. In many embedded tests such as for power amplifier, chip temperature is far beyond the room temperature, thus the knowledge of the ambient temperature of the detector is important to ensure accurate measurement. The bipolar transistor is inherent ideal device for temperature measurement in silicon processing. In DC measurement , if applying a bias current (I_n) n times that of the normal detector

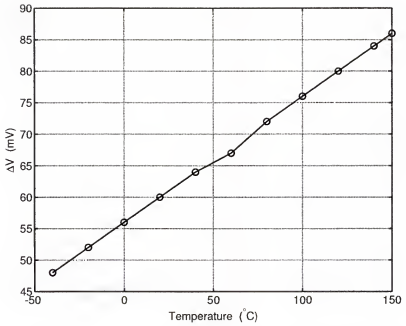


Figure 7–3: The simulated relationship of the output voltage (ΔV) versus temperature.

bias current (I_0) (switch S in Figure 7–2 is on), the base-emitter voltage is

$$V_{BE_n} = V_T \ln \frac{I_n}{I_S} \tag{7.5}$$

Subtracting the base-emitter voltage V_{BE_0} at bias current I_0, the voltage difference $V_{BE_n} - V_{BE_0}$ is

$$\Delta V = V_{BE_n} - V_{BE0} = V_T \ln n \tag{7.6}$$

Thus, the thermal voltage is

$$V_T = \frac{\Delta V}{\ln n} \tag{7.7}$$

where, n is usually a number between 10 and 20. With the known thermal voltage, the input signal strength can be predicted from the transfer curve at the specific thermal voltage or temperature, or using some other techniques. Figure 7–3 is the simulated

ΔV variation with temperature (n=10). It shows ΔV is linearly proportional to the temperature, as indicated by (7.7).

7.4 Measurement Results

The single-transistor detector is measured by turning off the on-chip current source and connecting an off-chip current source (20 μA) to the emitter of the input transistor Q_1 in the Meyer power detector. Figure 7–4 shows that the measured results are consistent with the simulation. Besides, the LNA monitoring circuit is tested with two single-transistor detectors. The extracted transducer voltage gain, voltage gain and input impedance are the same as the results in Chapter 5.

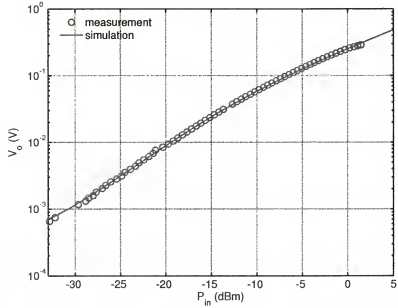


Figure 7–4: The transfer characteristics of a single-transistor detector.

7.5 Conclusion

Calibration-free detection circuit is needed in the embedded RF IC testing for practical application. The errors in Meyer power detector are analyzed from the

aspect of process variation, mismatch and noise, and then a single-transistor detector appropriate for embedded RF IC testing is proposed. This detector has the advantages of small chip headroom, process and mismatch independence, and ease to design. The emerge of this calibration-free detector makes the embedded RF IC test become feasible and practical by eliminating the costly or unpractical calibration procedure.

CHAPTER 8
SUMMARY AND SUGGESTIONS FOR FUTURE WORKS

8.1 Summary

This dissertation is concerned with the development of embedded RFIC test circuits. The detection theory on bipolar power detectors is analyzed in a closed-form. It shows that the bipolar power detectors have three signal detection regions (large-signal detection region, small-signal detection region and crossover region), and also are capable for RMS power detection when working in the small-signal detection region. Several power detectors were developed. Meyer power detector has the simplest structure but a large crossover region; the new power detector with voltage divider enhancement has a minimized crossover region and a 65 dB dynamic range; the RMS power detector extends the dynamic range by cascading several stage attenuators, and the demonstrated RMS detector can work with signals up to 20 GHz and has a dynamic range over $\geq$ 40 dB for RMS power detection; symmetric and nonsymmetric differential power detectors with high rejection to common-mode noise are developed and the nonsymmetric detector is used as a key component in a six-port reflectometer design.

Based on the success for the development of detection circuits, two practical applications for embedded test are demonstrated. The first one is a LNA monitoring circuit using two RF power detectors to detect the catastrophic faults or parametric faults for LNA production test. The algorithms to extract the transducer voltage gain, voltage gain and input impedance are presented and the measurement shows

the extraction using the power detectors is accurate. The LNA monitoring circuit takes at most 15% additional chip area and is the most cost-effective design nowadays. The second is a six-port reflectometer designed to measure microwave reflection coefficients. This compact monolithic six-port reflectometer consisting of a resistive power divider, a phase shifter and several power detectors, is the most area-efficient and cost-effective design for on-chip S-parameter measurement systems. The measurement shows the six-port reflectometer achieves high measurement precision which is comparable to the commercial network analyzer.

Besides, the calibration of the detection circuits is studied. The errors in Meyer power detector are analyzed from the aspect of process variation, mismatch and noise, and then a single-transistor detector design is proposed. The single-transistor detector has the advantages of small chip headroom, process and mismatch independence and ease to design. The emerge of this calibration-free detector makes the embedded RFIC test become feasible and practical by eliminating the costly calibration procedure.

8.2 Suggestions for Future Work

The ultimate objective of our research is to realize embedded test of RF system on chip. The successful development of RF power detectors has brighten the future of the embedded RF test. The detectors can be inserted on any nodes of interest in the RF transmitter or receiver. As shown in Figure 8–1, the nodes marked with a short arrow are the points where the detectors may be attached to diagnose the status of the system. The detector can monitor the antenna output, the LNA input and output, the mixer LO input, the PA input and output, etc. Usually the detectors with high input impedance are used because they have small disturbance on the RF system and do not bring much design complexity.

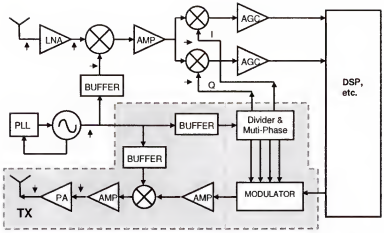


Figure 8–1: The detector placement in a transceiver.

In the embedded test of RF system, some functional blocks are needed to fulfill various embedded self-test functions:

1. On-chip microwave signal source

   Current RFIC test uses external microwave signal source to stimulate the DUT through cables and probes. The loss on the cables and probes must be calibrated by a lengthy and tedious calibration procedure. On-chip microwave signal source eliminates the necessity of the cables and probes, enables the parallel test for volume production and minimizes the test time. With the development of the calibration-free detector, the signal source output can be predicated accurately. The challenges of microwave signal source design are frequency tuning range, signal purity, chip headroom, and crosstalk if antenna is employed.

2. On-chip network analyzer

   Based on the principle of six-port reflectometer, two-port or multi-port on-chip network analyzer could be realized. However, if the network analyzer is used for

built-self-test, some design strategy must be used to minimize the process variation effect. The six-port network analyzer can be built in a microwave probe or in the device interface board (DIB). Thus, the distance between the network analyzer and the DUT is shorten, the test cost reduced and test efficiency improved.

3. On-chip spectrum analyzer

   A spectrum analyzer can be placed at the mixer output to detect the output spectrum. It provides another efficient means to diagnose the parametric or catastrophic faults in the RF system. Besides, the spectrum analyzer can also be built in a microwave probe or in the DIB.

4. On-chip switch

   On-chip switch can change the test path and improve the test efficiency. However, the insertion loss in the switch may degrade the performance of the RF system. Moreover, the variation of the insertion loss makes it difficult to use in practical application. Some techniques must be developed to calibrate the loss in the switch.

With the development of the above functional blocks, a RF system with complete embedded self-test funtions could be implemented.

APPENDIX A
CALIBRATION IN ONE-PORT MEASUREMENT SYSTEM

A.1 Determination of The Input Signal Level

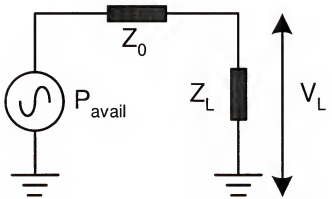


Figure A–1: Equivalent circuit of one-port measurement system.

One-port measurement system is represented as a signal source with source impedance Z_0 connected to load impedance Z_L in Figure A–1.

The power delivered to the load is

$$P_{load} = (1 - |\Gamma_L|^2) P_{avail} \tag{A.1}$$

where

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{A.2}$$

Rewriting (A.1) in terms of Z_L, Z_0 and P_{avail} gives

$$P_{load} = 4 \frac{Re\{Z_L\} Z_0}{|Z_L + Z_0|^2} P_{avail} \tag{A.3}$$

The average power delivered to a complex load for sinusoidal signals is equal to

$$P_{load} = \frac{|v_L|^2}{2} \cdot Re\{\frac{1}{Z_L}\} \tag{A.4}$$

Substitute (A.4) to (A.1), thus

$$|v_L| = \frac{\sqrt{8Z_0 P_{avail}}}{|Z_L + Z_0|} \cdot \sqrt{\frac{Re\{Z_L\}}{Re\{\frac{1}{Z_L}\}}} \tag{A.5}$$

A.2 Error Model for One-Port Measurement System

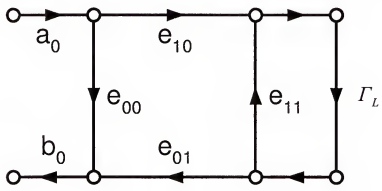


Figure A–2: Flow graph of the hypothetical error adapter for one-port measurement system.

The fictitious error-adapter network in Figure A–2 is only for one-port measurement system [54]. The left and the right planes of the two-port error adaptor represents respectively the reference planes of the coaxial cable and of the probe tip. The arrows visualize the signal flow in the error adaptor. a_0 and b_0 are the respective incident and reflected waves; a_1 and b_1 are the waves associated with the device under test. Four error terms are used to describe this error-adaptor network:

- Directivity error – e_{00} represents all the signals that are reflected before they reach the reference plane of probe tip.

- Frequency response errors – e_{10} and e_{01} represent the errors caused by an non-ideal transfer path between the reference planes of cable and probe tip.
- Port match error – e_{11} represents the reflected signal resulting from a non-ideal effective source impedance when looking back into the reference plane of probe tip.

The term e_{10} and e_{01} are usually used together as a product because the two terms cannot be distinguished from each other in the one-port measurement system.

The error terms can be obtained by the calibration with open, short and load standards [54]. The measured data on the reference plane of cable are

$$\Gamma_{C_{open}} = e_{00} + \frac{e_{01}e_{10}}{1 - e_{11}} \tag{A.6}$$

$$\Gamma_{C_{short}} = e_{00} - \frac{e_{01}e_{10}}{1 + e_{11}} \tag{A.7}$$

$$\Gamma_{C_{load}} = e_{00} \tag{A.8}$$

Solving (A.6), (A.7) and (A.8) gives the three error terms

$$e_{00} = \Gamma_{C_{load}} \tag{A.9}$$

$$e_{11} = 1 - 2\frac{\Gamma_{C_{load}} - \Gamma_{C_{short}}}{\Gamma_{C_{open}} - \Gamma_{C_{load}}} \tag{A.10}$$

$$e_{01}e_{10} = 2\frac{(\Gamma_{C_{open}} - \Gamma_{C_{load}})(\Gamma_{C_{load}} - \Gamma_{C_{short}})}{\Gamma_{C_{open}} - \Gamma_{C_{short}}} \tag{A.11}$$

The signals b_0 and b_1 in Figure A–2 are

$$b_0 = a_0e_{00} + a_1e_{01} \tag{A.12}$$

$$b_1 = a_0e_{10} + a_1e_{11} \tag{A.13}$$

Then the reflection coefficient on the plane of coaxial cable Γ_C is obtained as

$$\Gamma_C = \frac{b_0}{a_0} = e_{00} + e_{01}e_{10}\frac{\Gamma_P}{1 - e_{11}\Gamma_P} \tag{A.14}$$

or the reflection coefficient on the plane of the probe tip Γ_P is

$$\Gamma_P = \frac{a_1}{b_1} = \frac{\Gamma_C - e_{00}}{e_{11}(\Gamma_C - e_{00}) + e_{01}e_{10}} \tag{A.15}$$

The power delivered to the load P_{load} can be derived from the error model as follows. Rewrite (A.12) as

$$a_1 = \frac{b_0 - a_0 e_{00}}{e_{01}} \tag{A.16}$$

Then the power delivered to the load is

$$P_{load} = (\frac{1}{|\Gamma_P^2|} - 1)\left|\frac{\Gamma_C - e_{00}}{e_{01}}\right|^2 P_{avail} \tag{A.17}$$

Similarity, rewrite (A.13) as

$$b_1 = \frac{a_0 e_{10}}{1 - \Gamma_P e_{11}} \tag{A.18}$$

Thus

$$P_{load} = (1 - |\Gamma_P^2|)\left|\frac{e_{10}}{1 - \Gamma_P e_{11}}\right|^2 P_{avail} \tag{A.19}$$

These two load power equation are identical from the comparison of measurements.

APPENDIX B
Basics of Two-Port Networks

Although a network may have any number of ports, network parameters can be explained most easily by considering a network with only two ports, an input port and an output port, as shown in Figure B–1. The behavior of the two-port networks are often characterized using the z, y, h or ABCD parameters at low frequency. However, it is difficult to measure these parameters at higher frequency. The measurement of these parameters needs the input and output of the device to be successively opened and short-circuited. The required open and short circuits are difficult to achieve over a broadband range of RF frequencies. Moreover, the measurement at higher frequency usually requires to adjust tuning stubs for each measuring frequency. It not only makes the measurement inconvenient and tedious, but also may cause oscillation and make the measurement invalid.

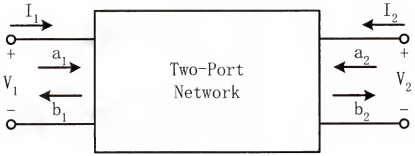


Figure B–1: Two-port network representation.

Scattering parameters (S parameters) are a set of parameters used in RF/microwave range for the characterization of the behavior of a two-port network. These parameters are defined in terms of traveling waves (a_i and b_i), instead of only terminal voltages V_i and currents I_i in Figure B–1. Therefore, S parameters can be measured on a device which is connected with the network analyzer through low-loss transmission lines. Besides, S parameters are usually measured with the device connected with 50 Ω source and load impedance and the risk of oscillation is small because the short and open circuits are not needed.

The fundamentals of S-parameter concepts are present in the following. Given an incident wave V^+ and a reflected wave V^-, the normalized incident voltage wave a and the normalized reflected voltage wave b are

$$a = \frac{V^+}{\sqrt{Z_0}} \tag{B.1}$$

and

$$b = \frac{V^-}{\sqrt{Z_0}} \tag{B.2}$$

where Z_0 is the characteristics impedance of transmission line. The voltage waves a and b can also be written in terms of V and I (peak values) as

$$a = \frac{1}{2\sqrt{Z_0}}[V + Z_0 I] \tag{B.3}$$

and

$$b = \frac{1}{2\sqrt{Z_0}}[V - Z_0 I] \tag{B.4}$$

The two-port network in Figure B–1 has an incident wave a_1 and a reflected wave b_1 at port 1 and an incident wave a_2 and a reflected wave b_2 at port 2. The representation

of this two-port network is given in the matrix form

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{B.5}$$

where S_{11}, S_{12}, S_{21}, and S_{22} represent the reflection and transmission coefficients.

From (B.3) and (B.4), the power delivered to any port i is

$$P_i = \frac{1}{2} Re[I_i V_i^*] = \frac{1}{2}|a_i|^2 - \frac{1}{2}|b_i|^2 \tag{B.6}$$

The chain scattering parameters (T parameters) are used in the analysis of cascade connections of two-port networks. The relationship of the input waves (a_1, b_1) and output waves (a_2, b_2) of the two-port network in Figure B–1 are defined as

$$\begin{bmatrix} a_1 \\ b_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} b_2 \\ a_2 \end{bmatrix} \tag{B.7}$$

For cascading networks, the overall T matrix is the products of T matrix of each stage.

APPENDIX C
The Measurement of Impedance

The impedance is originally defined as the complex ratio of the voltage to the current in ac circuits consisting of resistors, inductors and capacitors. Then, the impedance concept is applied to transmission lines and electromagnetic fields. The value of impedance may vary with the measurement plane and/or direction. Several types of impedance often used are listed as below:

- $\eta = \sqrt{\frac{\mu}{\epsilon}}$ is intrinsic impedance of medium.
- $Z_w = \frac{E_t}{H_t}$ is wave impedance.
- $Z_0 = \sqrt{\frac{L}{C}}$ is characteristic impedance.

Impedance measurements for transmission lines and electromagnetic fields are more complex than that in low-frequency lumped circuits. All the impedance measurements in the field are based on the following assumptions: the impedance variation leads to the superposition of the power waves a and b on the propagation line and the behaviors of the line change with the measuring planes. This is because the impedance can be deduced, provided that the power waves (a, b) and the behaviors of the line are known.

Usually, either one of the two following principles are used in the measurement of the propagating power waves and thus the impedance.

- part of the incident wave and/or emergent wave are coupled to measurement devices (for example, through a directional coupler)

- or the amplitudes of the waves along the propagation line can be measured with probes on several measuring planes.

The measurement devices for the propagating power waves can be a heterodyne- or homodyne-receiver, or a rectifier, or a power detector, or a high-speed oscilloscope.

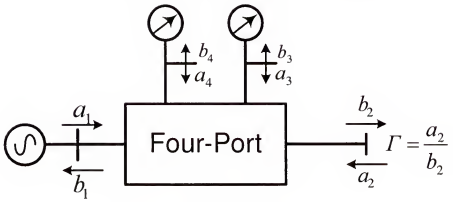


Figure C–1: Reflection coefficient measurement using a four-port junction.

Figure C–1 is an example of a device for measuring the propagating power waves. The device is a four-port junction with a signal source at the input port (port 1) and an unknown load at the measuring port (port 2). Assume the linear combination of the waves in the junction, the emergent power wave at the port i ($i = 1, 3, 4$) is

$$b_i = A_i a_2 + B_i b_2 \tag{C.1}$$

Thus, the emergent waves at the ports 3 and 4 are

$$b_3 = A_3 a_2 + B_3 b_2 \tag{C.2}$$

$$b_4 = A_4 a_2 + B_4 b_2 \tag{C.3}$$

The coefficients A_3, A_4, B_3 and B_4 are determined by the behavior of the four-port junction and they can be found by a series of calibrations of the junction. The

reflection coefficient of the measured DUT, $\Gamma = \frac{b_2}{a_2}$ is obtained by solving (C.2) and (C.3) if complex values b_3 and b_4 are measured with a receiver. This is the operation principle of the four-port network in commercial network analyzer.

However, it is much easier to measure the amplitude of the wave,

$$P_i = |b_i|^2 = |A_i a_2 + B_i b_2|^2 \tag{C.4}$$

The amplitude or power measurements simplify the hardware design. However, the calibration procedures become more lengthy and complex. The six-port techniques developed from this theory are simple for hardware design but have complex calibration. Before the review of the six-port theory, two other impedance measurement methods are introduced in detail.

C.0.1 The Slotted Line

A slotted line consists of a transmission line (usually waveguide or coax) with a ruler and a sliding probe. The sliding probe has an imbedded detector that allows the sampling of the electric field amplitude of a standing wave on the transmission line with a terminated load.

The standing wave ratio (SWR) on the line and the distance of the first voltage minimum from the terminated load on the line l_{min} can be measured with the slotted line. The magnitude and phase of the reflection coefficient are given respectively by

$$|\Gamma| = \frac{SWR - 1}{SWR + 1} \tag{C.5}$$

and

$$\theta = \pi + 2\beta l_{min} \tag{C.6}$$

where β is the wave number of the line. Thus, the complex reflection coefficient at the load is found from $\Gamma = |\Gamma| e^{j\theta}$ and the load impedance is

$$Z_L = Z_0 \frac{1+\Gamma}{1-\Gamma} \tag{C.7}$$

The slotted line was used to measure an unknown impedance at microwave frequencies. It has been substituted by the modern vector network analyzer because network analyzer has better accuracy, versatility and convenience. However, the slotted line is still used in some applications such as high-millimeter wave frequencies, etc.

C.0.2 The Vector Network Analyzer

The vector network analyzer is the most popular instrument to measure the S parameters of passive and active devices. The commercial products of the vector network analyzer operate up to 110 GHz and new multi-port network analyzers enable the measurement of three-port and four-port circuits. A simplified block diagram is shown in Figure C–2. The fundamental blocks include the directional coupler and several microwave receivers which are designed to process the magnitude and phase of the reference, transmitted and reflected waves from the network.

The directional coupler is a special reciprocal four-port network. For an arbitrary reciprocal four-port network that matched at all ports, its S-parameter matrix is

$$[S] = \begin{bmatrix} 0 & S_{12} & S_{13} & S_{14} \\ S_{12} & 0 & S_{23} & S_{24} \\ S_{13} & S_{23} & 0 & S_{34} \\ S_{14} & S_{24} & S_{34} & 0 \end{bmatrix} \tag{C.8}$$

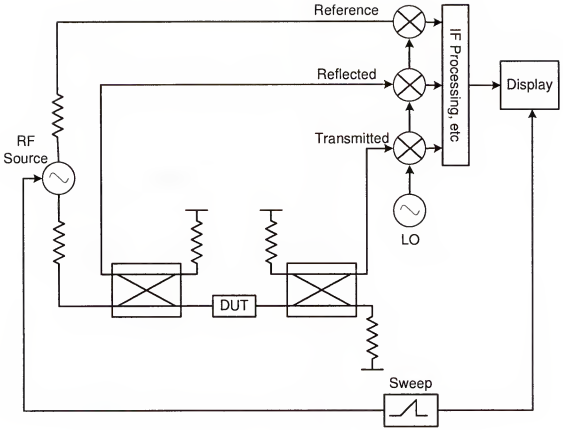


Figure C–2: Block diagram of a vector network analyzer.

For an ideal directional coupler, $S_{14} = S_{23} = 0$. The power flow in a directional coupler is shown in Figure C–3. The directional coupler is connected with a signal generator at port 1 and a device under test (DUT) at port 2. The input power enters port 1 and a fraction of the power is coupled to port 3 by the coupling factor $|S_{13}|^2$. The remainder of the input power then leaves port 2 to DUT with the coefficient $|S_{12}|^2$. Port 4 is an isolated port and there is only a terminator to absorb any waves of leakage. There are three quantities for the characterization of a directional coupler:

$$C = 10 \log \frac{P_1}{P_3} = -20 \log |S_{13}| \tag{C.9}$$

$$D = 10 \log \frac{P_3}{P_4} = -20 \log \frac{|S_{13}|}{|S_{14}|} \tag{C.10}$$

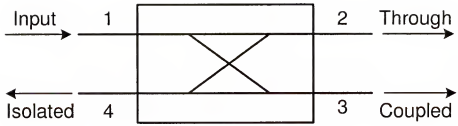


Figure C–3: Directional coupler symbol and power flow conventions.

$$I = 10 \log \frac{P_1}{P_4} = -20 \log |S_{14}| \tag{C.11}$$

The coupling factor $-$ C is the fraction of power entering port 1 that is coupled to port 3. The directivity $-$ D and isolation $-$ I is a measure of the coupler's ability to isolate forward and backward waves. The directivity of a coupler can be measured using a sliding matched load.

As shown in Figure C–2, the incident, reflected and transmitted waves are separated by the directional coupler, downconverted to IF band, and then sampled and processed by an internal computer. The magnitude and phase of the S parameters are shown on the display. Some other quantities such as SWR, impedance, group delay, etc can be derived from the S parameters.

The behavior of a directional coupler varies with frequency as well as the other components in the vector network analyzer. These variations must be determined by measuring some known standards with high precision. The procedure of the measurement is called calibration. Some error models [54] are built by calibration and used to correct the systemic error in the measurement.

APPENDIX D
Six-Port Calibration

The popular calibration procedures for six-port reflectometer are shown in Figure D–1. First, the off-line or in-situ characterization is employed to find the characteristics of power detectors used in the six-port. Then, the initial values of w_1, w_2, Z and R for the six- to four-port reduction are estimated. Next, the six- to four-port reduction procedure is to find the optimum values for the parameters in W plane. Finally, some well-defined standards are measured to find the coefficients in the bilinear "error box" transformation between the Γ plane and the W plane. In the following, the six- to four-port reduction technique is explained first, followed sequentially by the "error box" transformation, initial estimation and the characterization of detectors.

D.0.3 Six- To Four-Port Reduction

The six-port reflectometer requires eleven coefficients determined by some calibration. In contrast, the four-port reflectometer requires only six coefficients. Based on the four-port theory, Engen developed an approach to do calibration in two distinct steps. First, the six-port reflectometer is reduced to equivalent four-port reflectometer. This requires a determination of five of the eleven coefficients in the description

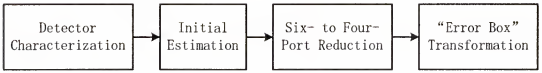


Figure D–1: Calibration of the six-port reflectometer.

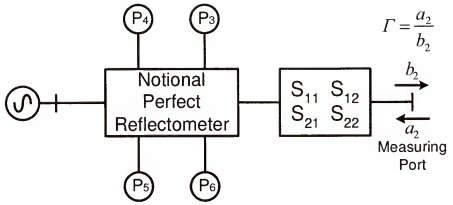


Figure D–2: Partitioning the six-port reflectometer.

of the six-port. Second step is to characterize the equivalent four-port and determine the remaining three complex coefficients. Figure D–2 illustrates the six-port is partitioned into a "perfect" four-port reflectometer and a two-port network whose S parameters characterize the "error box" transformation [55,56]. The notional perfect reflectometer is defined in W plane by five "reduction" coefficients (three scalars – w_1, Z, R and one complex – w_2). The reduction from six-port to four-port is given by

$$Q_4 = |w|^2 \tag{D.1}$$

$$ZQ_5 = |w - w_1|^2 \tag{D.2}$$

$$RQ_6 = |w - w_2|^2 \tag{D.3}$$

where w is the reflection coefficient in W plane and Q_i is $\frac{P_i}{P_3}$, the measured power at port 4, 5 and 6 normalized respectively by the power at the reference port 3.

Engen [51] has shown that the variable w can be eliminated from (D.1) to (D.3) and a constraint equation may be formed as

$$\begin{aligned} &AQ_4^2 + BZ^2Q_5^2 + CR^2Q_6^2 + (C - A - B)ZQ_4Q_5 \\ &+(B - C - A)RQ_4Q_6 + (A - B - C)ZRQ_5Q_6 + A(A - B - C)Q_4 \\ &+B(B - C - A)ZQ_5 + C(C - A - B)RQ_6 + ABC = 0 \end{aligned} \tag{D.4}$$

where

$$A = |w_1 - w_2|^2 \tag{D.5}$$

$$B = |w_2|^2 \tag{D.6}$$

$$C = |w_1|^2 \tag{D.7}$$

(D.4) is used as the basis for the six- to four-port reduction. It represents a quadric surface if (Q_4, Q_5, Q_6) denotes a point in a three-dimensional "Q space". A reasonably good initial estimation of the reduction coefficients may be obtained by observing the six-port response to a set of arbitrary loads. The reduction coefficients are then improved by iterating (D.4) with a least-square technique.

With the five reduction coefficients and the power meter readings, the reflection coefficient in W plane can be calculated [51]. The reflection coefficient is

$$w = u + jv \tag{D.8}$$

where

$$u = \frac{Q_4 - ZQ_5 + |w_1|^2}{2|w_1|} \tag{D.9}$$

$$v = \frac{Q_4 - RQ_6 + |w_2|^2 - 2uu_2}{2v_2} \tag{D.10}$$

u_2 and v_2 are the real part and imaginary part of the reduction coefficient w_2.

D.0.4 Bilinear "Error Box" Transformation

The bilinear "error box" transformation is the mapping of the reflection coefficient from W plane to Γ plane. The representation of the bilinear transformation is

$$w = \frac{a\Gamma + b}{c\Gamma + 1} \tag{D.11}$$

This bilinear function maps circles to circles. So, the measurement of loads with a constant absolute value of Γ will be on a circle in the W plane. With the known reduction coefficients from the six- to four-port reduction, the three complex coefficients a, b and c can be found easily by observing the six-port response to three known loads and solving the resulting three linear equations. Many other methods for calibrating the "error box" transformation are reported in the literature [57–59]. For example, *Kása* proposed a method to use one known load together with two different sliding terminations [57]. In our experiment, we use the open, short and load terminators to calibrate the "error box" transformation. It is the same as the SOL calibration for the commercial automatic network analyzer.

D.0.5 Initial Estimation

The iterative solution on (D.4) requires good initial estimation of the five parameters (three scalars Z, R, w_1 and one complex w_2). Various methods for finding initial estimates for the six- to four-port reduction were reported in the literature [51–53,60]. Engen's method [51] uses nine or more completely unknown but well-distributed loads in contrast to five loads required in the other three methods proposed by Stumper [52],

Neumeyer [60] and Wiedmann [53]. Stumper's method assumes that the five reflections are of magnitude 1 with different known phases. Neumeyer's method requires five reflections of equal but unknown magnitudes and unknown phases. Like Stumper's and Neumeyer's method, Wiedmann's method uses five reflections with unknown but constant magnitudes and unknown but well-distributed phases and can improve the accuracy in case where the other methods may become "ill-conditioned".

Stumper's method is used to find the initial estimates for our six-port reflectometer. Six loads with constant magnitude 1 but different known phases are realized by a sliding short. However, due to the loss in the probe and cable, the magnitude of the reflection is less than 1. Therefore, Stumper's method is modified by changing the magnitude of reflection from 1 to a known value (less than 1). The detailed algorithm in Stumper's method can be found in [52].

D.0.6 Characterization of Detectors

The process variation results in the variation of the detectors' transfer characteristics. Thus, the detectors must be calibrated to ensure the high-precision performance of the six-ports.

The power detectors used in the six-ports can be calibrated individually, outside the six-port network, or they can be calibrated in-situ without disconnecting them from the network. The detectors in the integrated six-port reflectometer must be characterized in-situ because the detectors are integrated and can not be disconnected. Three in-situ calibration methods are reported in the literature [61–63] and they respectively require to use one of the tools: power meter, variable attenuator

and multiple loads. Among them, the last one using multiple loads is the most convenient and effective method. So, this method is used to calibrate the bipolar power detectors in our six-port reflectometer.

For the in-situ calibration, an input signal source is connected with the six-port input (port 1) and a number of unknown loads are connected sequentially at the measuring port (port 2). The detectors' responses in the six-port are observed by varying the input power level. The transfer characteristics of a given detector can be expressed by

$$P_i = K_i v_i^{f_i(v_i)}, \quad i = 3, 4, 5, 6 \tag{D.12}$$

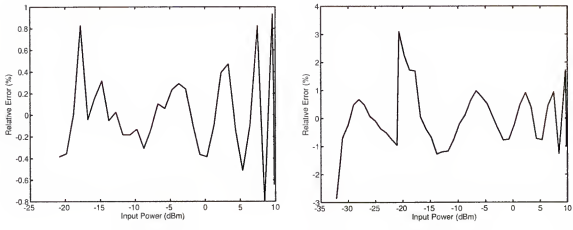
with

$$f(v) = 1 + b_1 v + ... + b_n v^n$$

$$v = \xi(v - v_0)$$

where P_i is the incident power, V_i the detector output voltage at port i, V_0 the detector output voltage when $P = 0$ and ξ a scale factor. (D.12) has been successfully used in the characterization of diodes. It may also be suitable to characterize the bipolar detectors. Figure D–3 is the relative fitting errors between the measurement data and the fitted curve from (D.12) with the order $n = 9$. It is seen the errors are $< 0.9\%$ when fitting from -20 dBm to 10 dBm and $< 3\%$ when fitting from -32 dBm to 10 dBm. Figure D–3.(a) also shows that, similar to the diode detectors, the bipolar detectors have the optimum fitting region roughly between -20 dBm and 0 dBm.

(D.12) can be applied to any detectors in the six-port reflectometer. Thus, for a given load Γ_k connected at the measuring port, the power ratio at port i can be



(a) (b)

Figure D–3: Relative fitting errors over different input power region

written as

$$L_{ik} = \frac{P_i}{P_3}\bigg|_{load_k} = \frac{v_i^{f_i(v_i)}}{v_3^{f_3(v_3)}}, \quad i = 4, 5, 6 \tag{D.13}$$

The ratio K_i/K_3 is not considered in the detector calibration because it is included in another six-port parameter known from calibration [63].

Taking the logarithm of (D.13),

$$\begin{aligned} &-\log L_{ik} + b_{1i} v_i \log v_i + \cdots + b_{ni} v_i^n \log v_i \\ &-b_{13} v_3 \log v_3 \cdots b_{n3} v_3^n \log v_3 = \log v_3 - \log v_i \end{aligned} \tag{D.14}$$

In our calibration, L unknown loads ($L = 5$ to 7) are used and the input power varies from -22 dBm to 2 dBm with a step of 0.5 dBm. Thus a set of linear equations are obtained from (D.14) and can be solved for the unknown $L_{ik} (k = 1, \cdots, L,$ $i = 4, 5, 6)$ and $b_{ni} (i = 3, \cdots, 6)$. Due to the errors in the practical measurement, the technique for minimizing the mean square error is used to solve the linear system.

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